

Design Rules for Real Patterns

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Abstract

The purpose of this paper is to name and discuss some of the most basic issues in today's optical microlithography, promoting industry consensus and, specifically, definition of the industry standard Patterning Design Rules (PDR), that is, Design Rules for "patterns as built". Dimensional metrology for seamless PDR compliance is discussed, highlighting the issues at design hand-off from CAD to pre-tapeout validation and from validation in software to validation on wafers. Some of the gaps in validating the accuracy of patterning models used at design and pre-TO validation are identified, along with a proposal of how to bridge them. It is expected that, as our industry migrates from CAD based DR definitions to PDRs that reflect realities of microlithography at low k_1 , a complete self-consistent dimensional metrology infrastructure [1] will eventually be built. This is what will hold together compliance at design and on wafers, with model based WYSIWYG (what you see is what you get) design and process integration environment of the future.

1 Introduction

The need to decrease critical dimensions (CD) of the most advanced microelectronics devices increasingly challenges our views of the practical limits in optical microlithography. Proliferation of "sub-wavelength" optical lithography has obsoleted WYSIWYG paradigm in layout-to-silicon feature replication. Reticle-based image/pattern enhancement techniques (RET) enabled reduction of the largest systematic intra-field errors. Such changes to "as designed" pattern (on reticles) improved device performance and yield, extending processing margins achievable with optical lithography. Improved size tolerance, in turn, made it possible to print smaller devices. Yet, our industry's slow acceptance of the new design, patterning, and processing methodology is a factor in delaying introduction of the significant potential technology gains. Slow acceptance of aggressive RET is, to be sure, largely a reaction of the design, integration and test/yield communities' apprehension of the risks inherent in rapid proliferation of any new technology.

RETs, especially computer based aggressive modification of design can take such risks to an extreme. Numerous accounts of patterning failures and marginalities are found in the recent literature. Even a cursory review of the recent publications at SPIE Microlithography and Photomask meetings highlights many RET applications

that should be classified as something that is between sophisticated frills and demonstrably wasteful changes of the design DB. ISQED 2002 Panelists reflected on the gap between those who strongly advocate an EDA-lead changeover of design and manufacturing practices, and business models, vs. the practitioners of microelectronics manufacturing who take proposals to extend the envelope of our POR (process of record) with a grain of salt. When asked, they may comment on the rate of change being too fast, insisting on elaborate risk assessments before they are convinced. Recent industry survey of the systematic non-particle functional bin losses [2] identified a trend for reduced technology-limited yield in CMOS, as it evolved from CD ~ 500nm to 180nm. This suggests that multiple accounts of the isolated cases of failure due to weak links in design and integration of patterning may be a part of a much broader trend, implicating a growing deficiency of our design and integration practices, and PDR validation.

We may well be violating every DR there is, but we do not know that – not on 100% of such instances. The reason is simple: we have long run out of DRs that are applicable realistic patterning and of the capability to sufficiently validate them. Today's validation – the first time a patterning issue is noticed – often is device yield.

This paper reviews basic definitions in dimensional metrology and how we use dimensional metrology (and functional test based data) to design OPC or other RETs. It names a small set of generic Patterning Design Rules, with dimensional metrology capabilities required support them, and goes through in-depth review of one of them.

Dimensional metrology infrastructure of PDR validation (missing today), design/function-based metrology and appropriate metrics of compliance can support the model-based WYSIWYG design and integration environment. This is a solid foundation for "deep sub-wavelength" patterning and efficient microelectronics manufacture.

2 Digital ICs, Lithography and Design Rules

Digital ICs may be the most commonly manufactured microelectronic products of today. Microlithographic patterning of ICs, on the other hand, retained many similarities with analog (objects and their recorded images are of continuous tone, with infinitesimal variations of tone, size and shape) microphotography of 1950s. The built-in expectations of product requirements,

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materials properties, processing and manufacturing environment are hundreds years old.

Required to be either fully ON or OFF binary devices are relatively forgiving of manufacturing tolerances. This property enables an efficient mass-production of high yield/performance products that are both reliable and inexpensive. The tightest tolerance required is in matched transistor pairs, preventing the circuit lock-up and/or inappropriate change of state. This requirement is served by symmetry-based (translation, mirror, point) cell replication in IC design, instancing. Efficient IC manufacturing is only possible when every its aspect maintains symmetries required by devices.

If an IC were just a massive array of near-perfect transistors, it would be easier to make. But, to provide complex functions, IC must generate its own pulses to many registers' triggers, amplify and invert signal etc. Transistors that serve such functions are much less numerous, but, because they are designed to match multiples of other devices, their being built to size is also critical. The further away one device is from another, the less matched they may be without any losses. All devices in a die are sized and toleranced according to their design/function. Sizing requirements, reflected in Pattern Design Rules, repeat on the next die – from matched pairs to circuit neighbors, small vs. large etc.

Imaging with optics, unlike patterning with many other means, is a nearly perfect match for the need: imaging properties change slowly as the function of distance, that is to say, locally translation invariant. Unfortunately, all other symmetries of optical imaging systems are broken by aberrations, illumination and polarization effects. In-plane image vibration during exposure on scanners is just one detractor in the loss of isotropic (X same as Y) imaging. In order to make devices that rely on more than local translation invariance, all optical lithography systems are designed, built and maintained as free of errors as possible. Optical microlithography enables manufacture of devices that are near- perfectly matched over small distances and very well matched over the whole field. Any device features on the reticle, either isolated or in uniform arrays with period $>\lambda/2NA$ are replicated with near-perfect uniformity (low variance).

Simultaneously correct sizing of both small and large features, on the other hand, is somewhat difficult due to optical diffraction and interference effects. Significant variation occurs for features in varying proximity of each other and at the end of a uniform array $>\lambda/NA$ distance is required (wasted) to either prevent or compensate such changes in imaging. To sum up: optical lithography may be the perfect match for the manufacture of uniformly sized and spaced devices. At its incoherent cut-off limit,

it allows printing close to one device per $(\lambda/2NA)^2$ area on the wafer. Optical microlithography at 248nm (in air/no frequency doubling) can pattern devices at half-pitch of 64nm, with device CD being much smaller.

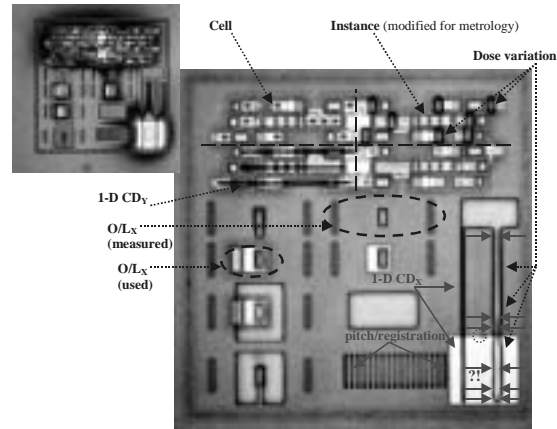


Figure 1. Metrology Test Site in bright field with (insert) NA=0.2, $\lambda=546\pm 5$ nm and NA=0.9, white light.

Printing on the previously patterned substrates, illustrated in Fig. 1 [1], may degrade device replication by optical lithography or it may retain it, if at a price. It may also be quite forgiving of error (self-compensating), precluding accrual of sizing errors in device patterns. The outcome is a strong function of layouts and patterning processes.

Prevailing design and manufacturing practices of today severely limit the ultimately achievable device tolerances by requiring that all features – any shape, size, polarity, orientation, regardless of proximity – be printed “to size”. Although much better patterning and device performance can be achieved through design and process integration, limitations of this kind are not obvious at design, let alone what it will cost to manufacture “as designed” or what gains we lost by failing to explore alternatives.

To better account for actual device needs, reducing waste inherent in indiscriminate requirements for tight sizing, as well as losses of performance and yield wasting resources of the superfluous rather than driving tighter tolerance in something critical, we need **design- and function-aware Patterning Design Rules**. These Rules must be based on the designers' knowledge of the design/device function. They must also account for patterning processes, with our ability to control process and assure compliance. It is of essence to all of us to understand them, and all aspects of IC manufacturing embodied in them, from basic physics to trade-offs in performance and yield, manufacturability, costs etc. Improving device tolerances assigned to such PDRs, as well as improving PDRs themselves, is the path that leads to the emergence of the superior IC design and manufacturing methodologies.

3 Design Rules and Dimensional Metrology

Design Rules is a normative document that specifies the key dimensions of a product that may be manufactured, while staying within known capabilities of a generation of lithography and patterning equipment, supported by everything required to produce an IC – from design and design validation methods and tools, to materials and processing, metrology and process control, failure analysis etc. *Design Rules* is our collective acceptance of what are (rather, used to be) the *most essential properties of a design*. DRs may look less than glamorous, but when each DR requirement is obeyed at design and compliance is validated, gross patterning deficiencies are unlikely. A product may be designed, design can be validated and chips be manufactured - with product properties predictable and close to the expectations. As in any well-run *business process*, value ranges expected for each single Design Rule are reviewed in the light of all recent learning. New value or tighter range of a Design Rule values may be needed to preclude marginal designs that lead to yield loss. Design Rule is relaxed when it is established – with certainty – that the losses of anything tangible do not occur when it is exceeded, especially when relaxing this Rule leads to quantifiable tangible gains or to the recognizable non-tangible gains.

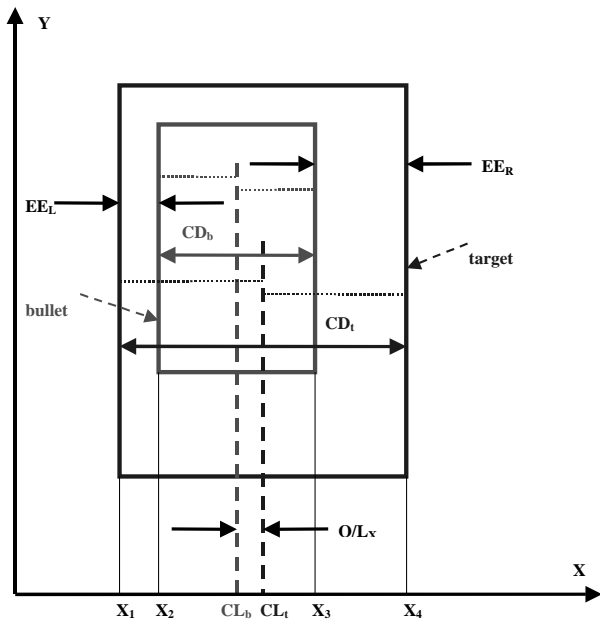


Figure 2. Linewidth (CD), centerline (CL), overlay (O/L) and edge-to-edge overlay (EE O/L).

To define Design Rules, Patterning Design Rules and their counterparts in the dimensional metrology, we use broadly applicable convention [1, 3-5] illustrated in Figure 2. We use the name feature to denote the simplest element in one layer of the design of a thin film device. Feature linewidth (space width, width, critical dimension or CD) in layer t (target, reference) and level b (bullet,

resist, current) is denoted CD_t and CD_b , respectively. If the edge coordinates are denoted as X_1 , X_2 , X_3 and X_4 , then

$$CD_t = |X_2 - X_3|$$

and

$$CD_b = |X_1 - X_4|.$$

Likewise, the centerlines of the target and bullet features are denoted CL_t and CL_b ,

$$CL_t = (X_2 + X_3)/2$$

and

$$CL_b = (X_1 + X_4)/2.$$

Since microlithography involves patterning very many features in each layer, a set of all centerline coordinates, registration, is of interest when it pertains to in-plane distance between a centerline of a feature in one layer and a feature in another layer, used as reference. This distance is centerline overlay (overlay, O/L). Referring to Fig. 2, overlay of two features, whose centerlines are CL_b and CL_t , is defined using the following convention:

$$O/L = CL_b - CL_t.$$

PDRs require that certain widths in certain features be within stated allowed ranges, manufactured to size within stated tolerances. Accurate account for EE O/L is required for effective design and integration of IC patterning. Failures to comply with EE O/L PDRs in back end of the line (BEOL, metallization) are known to lead to poor yield and reliability. Metrology of device O/L and EE O/L illustrated Fig. 1 was developed [6]. It is on SIA and SEMATECH Roadmaps since 1994. Yet, in today's practice, device level O/L, especially EE O/L, is seldom measured [7]. Designers' assumption that dimensional metrology is readily available and used to validate PDRs, as used at design and pre-TO validation, is violated.

Today's design environment still has, or appears to have, a complete account of all dimensions of all features in all layers. Design and integration universally recognize that "over-design" leads to lower profits, that "under-design" is a risk that may result in loss of product yield and/or reliability. We know that the best-designed product does not fail at "a single weak link" – it does not have one. When stressed to fail, the best-designed product will fail everywhere at once, reaching the highest stress limit. To achieve that, our design practices shrewdly prescribe where the tightest DRs may be used. Designs are thoroughly evaluated to make sure that if the tightest DR is used in just a few layouts of a product, these be re-designed and relaxed or the rest of the product also take full advantage that stems from using that tightest DR. Yet, our design and design validation environment is largely oblivious of the diverse environments in imaging, image recording and image transfer for one layer on a virgin substrate, let alone on a previously patterned and processed wafer. Assumption that the design is uniformly

replicated on the wafer and that the product is compliant with the design, within tolerance, is no longer true.

Low k_1 optical microlithography brought in strong new interactions of imaging and patterning processes with design. This patterning environment is deluged with unintended variations of both CD and image placement: image placement of dissimilar features is not the same, asymmetric aberrations and illuminator errors move image laterally through focus, errors of OPC or assist features, of phase, transmission, size or placement of phase shifters result in variations of both CD and image placement. What may be the least recognized is that potential improvements of pattern tolerances and process windows, the goal of RET, are only possible to the extent that their integration may reduce the total of all patterning errors. The success or failure of microlithography is not dependent on improved image “resolution” or “fidelity”. That is predicated by sustained reduction of CD and EE O/L tolerances in device patterning, as required by PDR, on the condition that it is the most cost-effective means to improve product yield and performance.

It is of essence to all of us in microelectronics industry to review and define a set of generic Patterning Design Rules, to make certain that they are supported by a complete set of dimensional metrology tools uniformly applicable at every step of model-based evaluation of design and validation of compliance – from database to wafers:

- ◆ models of patterning whose accuracy is known for all PDR cases and easily validated in layouts;
- ◆ function-aware metrology for design assessment and pre-TO compliance validation;
- ◆ function-aware metrology for post-TO and in-production PDR compliance validation;

Referring to critical layers in CMOS and bipolar ICs, here is a short list of generic PDRs:

One-layer Design Rules

- ◆ **linewidth** or **space width** (in 1-D and 2-D features), with MAX and MIN; between opposing edges in one layer;
- ◆ **area** of 2-D islands or trenches, with **perimeter** and **aspect ratio**; possibly, radius of corner rounding.

Two-layer Design Rules

- ◆ **Edge-to-Edge overlay**, distance between two edges (same or opposite, with MAX or MIN) in layer pairs;
- ◆ **Area of overlap** for 2-D features in layer pairs (area that is common to both layers).

4 PDR case study: 2-D feature (emitter or contact)

This is an illustration, and discussion, about what is and is not important in patterning ICs. It highlights the key aspects of model-assisted design environment in the case of the simplest serif-based OPC [8]. This OPC is commonly used at contact, via and implant layers, as well as emitter of bipolar devices. This old example has no proprietary aspects and is exceedingly simple, making it easy to observe and discuss the issues.

Problem statement:

Rectangular and substantially isolated emitter openings fail to print to size across all emitter sizes allowed by the Groundrules. When exposure is such that large rectangles are “on target”, rectangles with smaller side $< \lambda/NA$ are undersized; percentage area loss is the worst for squares. Since the sidewall narrowing technology is used to shrink emitter area, this poor size tolerance is applied to a much smaller effective emitter area. Bipolar transistor design and PDRs of relevance are illustrated in Figure 3; a great deal of salient detail related to these generic DRs is available in the public domain [9]:

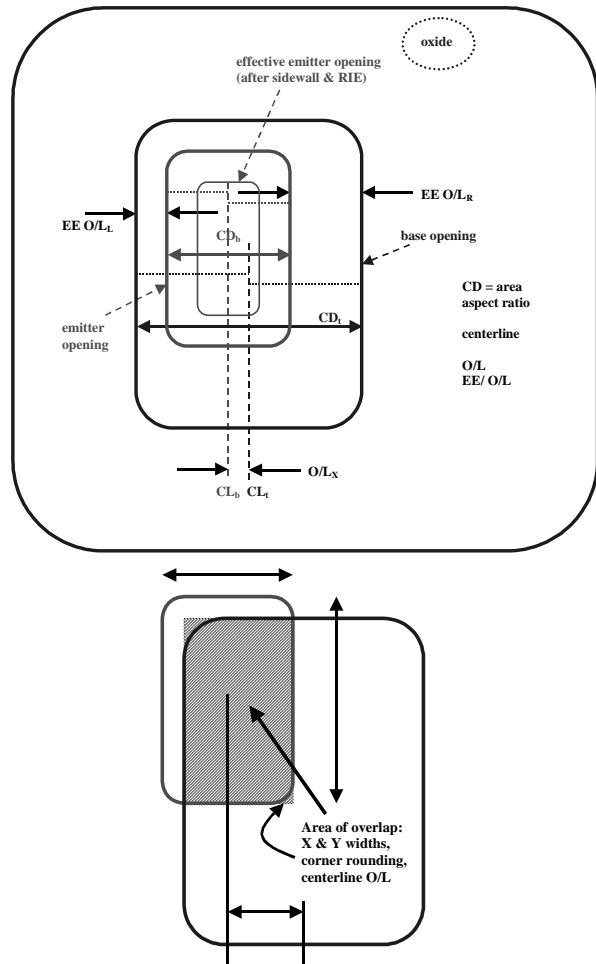


Figure 3. PDRs for emitter opening in bipolar transistors. Design is Fig. 2. Printed resist patterns shown in Fig. 1.

Design #1: non-aggressive serif

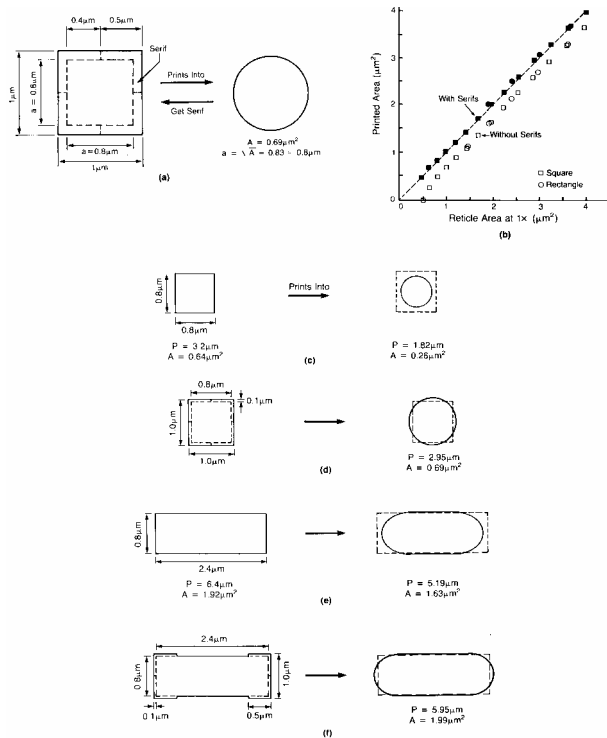


Figure 4. Design and properties of non-aggressive serif.

Although designers **want** emitter printed as a rectangle with **aspect ratio** ~ 1.5 (for performance transistor be fast, driving as high a current as allowed by current density), they **need** to get all emitters built close to **designed size**, with tight control of **conductance** for **all sizes** and **types**.

Quest for best RET (introduction to dialog):

What is “optimal design”? What is “designer intent”? What are design objectives? How should the many conflicting requirements be co-optimized?

A square is the **least complex shape** on the design grid. A model of lithographic printing shows that a single size square serif gives some improvement of areas printed for rectangles across a broad range of sizes and aspect ratios, as needed. This is a two-parameter design (serif size and extension/jog). It involves one or two experimental data points and a “back of the envelope” design procedure and model-based assessment of variable of area, perimeter and aspect ratio correction at “aggressiveness”; Figs. 4-5.

Design must be validated - the means may not exist. Which design is easier to manufacture on the reticle?

Model-based evaluation of impact, such as influence of mask sizing error on sizing in print and on defect printability: the more aggressive serifs, the stronger impact.

Design #2: aggressive serif

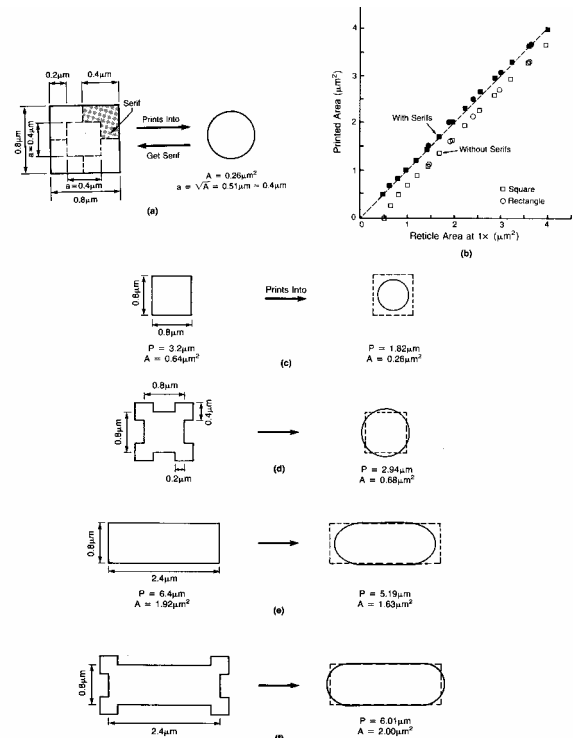


Figure 5. Design and properties of aggressive serif.

Which design gives the least error of size to target?

Which design gives the least variance for each size?

Both aggressive and non-aggressive design result in print area, perimeter and aspect ratio brought up to near target for all features. **But...** aggressive design has poor process windows, driving high variance (Fig. 8).

Which is a better design?

What are the metrics?

Is the model accurate?

How accurate is metrology?

Need metrology of area, perimeter and aspect ratio.

This is the DR at stake here – better control of this parameter, **area**, indicates success. Build and print reticles (POR). Measure area in print, Figs. 7, 9-10. Use estimated error to improve the design. Correct inaccuracy during model use in RETs (and model-based pre-tape-out validation). Dimensional metrology (of area in print) and electrical test data (cross-checked and self-consistent) - not the model - are the inputs to model-based design procedure (rule, algorithm).

Pre-T/O design validation requires accurate models.

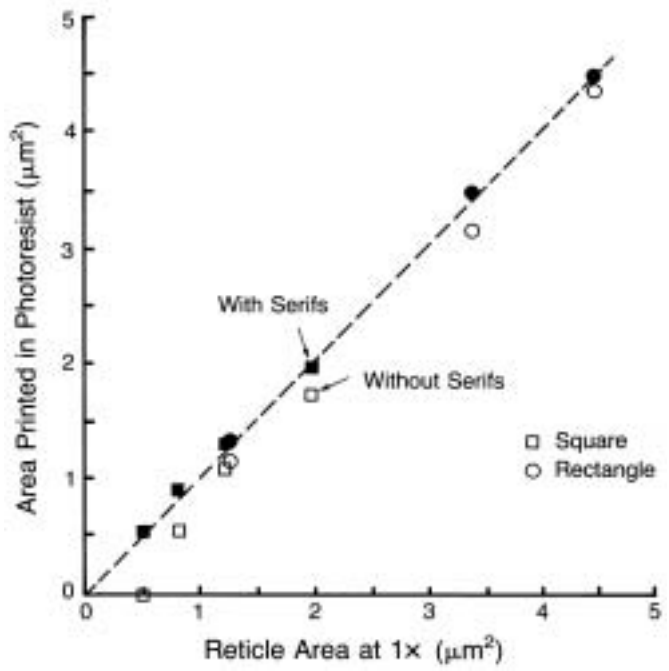
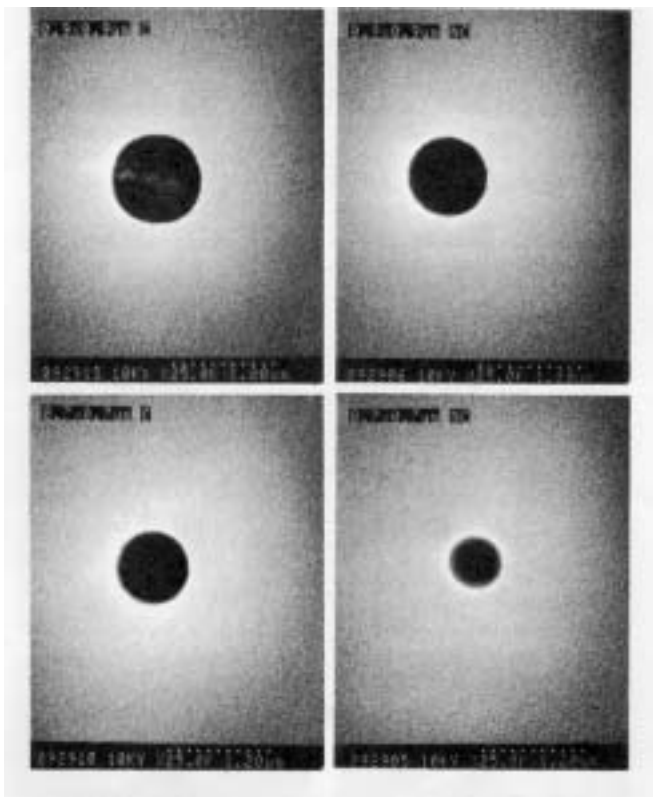
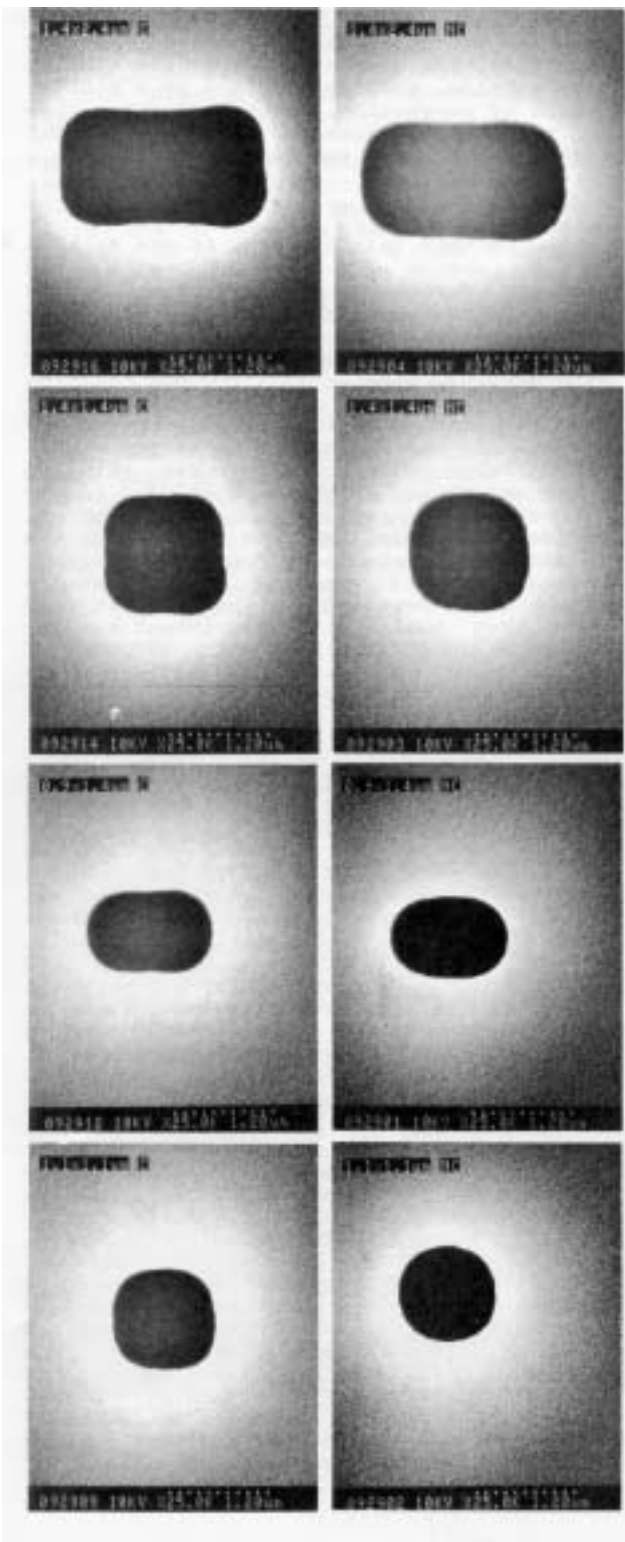


Figure 7. SEM based metrology of area in print.

Post-tape-out design validation requires metrology.

Metrology of area done with a specially modified SEM [6] confirms (Fig. 7) that emitters with serif corrections print closer to target area and aspect ratio across a wide range of sizes and aspect ratios. This was laborious, not all PDRs were checked - poor capability. More is needed: show better process margin, performance and reliability.

Dimensional metrology of emitter size in Fig. 7 and, more to the point, **e-test of effective area** in Figs. 9-10 confirm that emitter openings with serifs print closer to target and (even) with improved distributions.

This is just begins to validate the utility and PDR compliance for isolated small 2-D features...

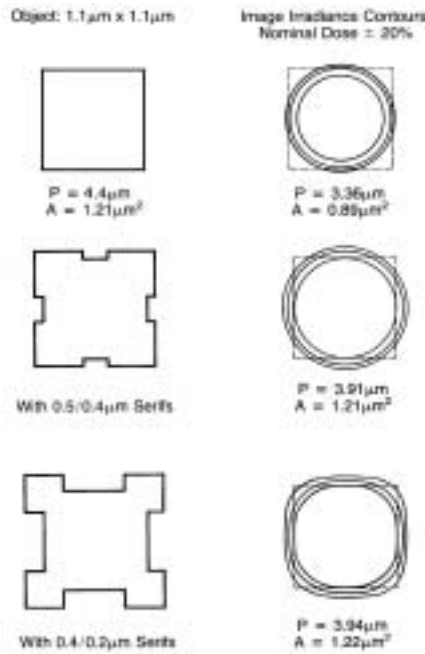


Figure 8. Engineering trade-offs in aggressive serifs.

5 Summary and Recommendations

Standard definitions of PDRs do not exist and, as the result, dimensional metrology capabilities to support them as required in low k_1 patterning do not exist, either.

CD-SEM based metrology of area in 2-D features with aspect ratio near 1:1 has been recently introduced. Their perimeter (PDR for storage node) still is not measured. Metrology of the smallest linewidths and space widths (the smallest distance edge-to-edge in opposing edges) in layouts is still manual and tedious. Validation of device O/L, EE O/L and overlap is handicapped by the lack of dimensional metrology infrastructure [1, 3, 5, 10, 11].

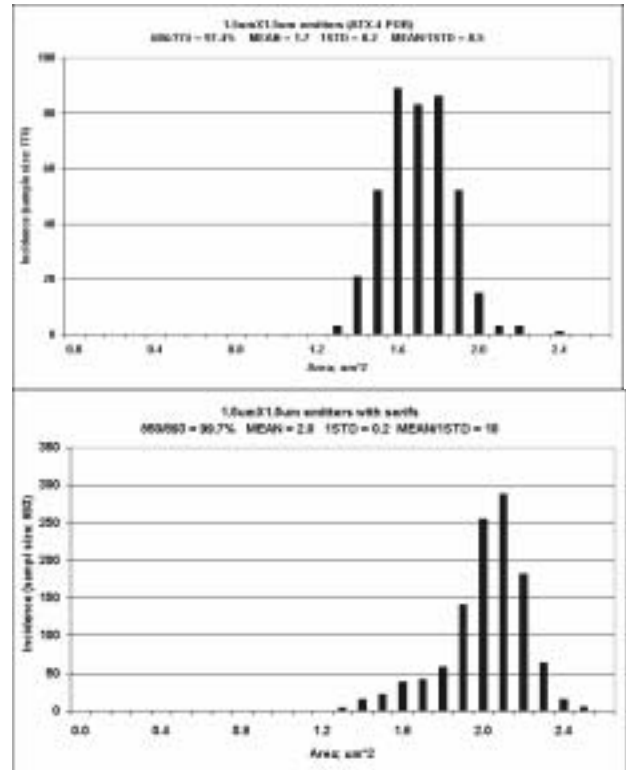


Figure 9. Large emitters with serifs are closer to target and tighter distribution (mean/STD).

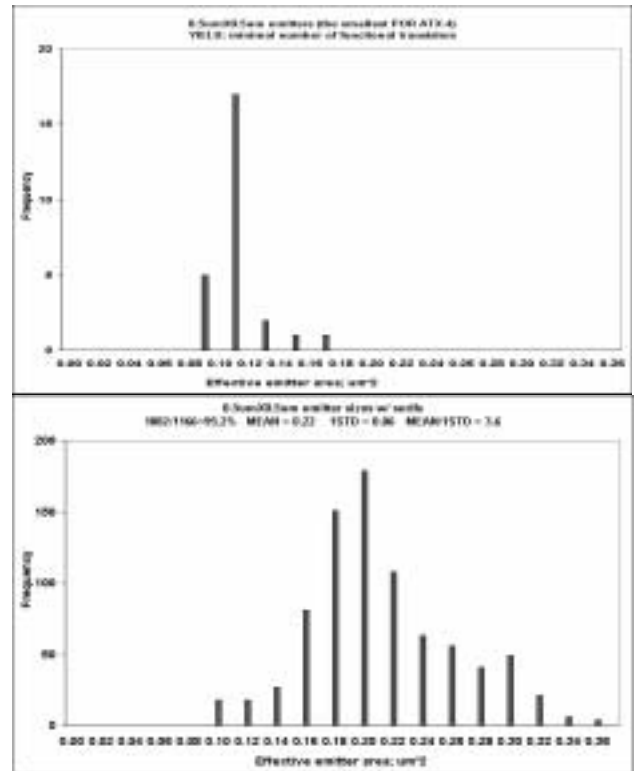


Figure 10. Small emitters without serifs are grossly below size and failing.

Functional test based assessments of patterning [12] point to significant systematic intra-field errors due to design and manufacture. Is yield the best way to validate PDRs?

PDR based dimensional metrology in model images and on wafers is required for sustained improvement of competitiveness and health of our industry.

Required dimensional metrology can be developed.

Effective dialog between designers, lithographers and metrologists is needed to arrive at consensual definitions of Patterning Design Rules. This paper is an invitation for colleagues to get active in PDRs and PDR compliance, to discuss the gaps in the leading technology forums and to publish our emerging consensus in the open domain. This author, with several colleagues joining, plans to take the subject of dimensional metrology for compliance to In-Depth Seminar at Microlithography 2004, like [13].

Our involvement with the suppliers, co-developing the new standard PDR-related dimensional metrology, may then take place at our industry's microlithography and metrology meetings. This will help the extensions of CD-SEM and CD-AFM metrology to emerge, fuel the development of the calibrated patterning/processing models to account for 2-D and 3-D patterning in microlithography and the emergence of the process-aware model-based metrology-assisted WYSIWYG paradigm for design and integration.

Acknowledgments

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