

Vertical Benchmarks and the CMUDSP



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CAD Benchmarks



- Good research requires good benchmarks
- CAD Benchmarks \approx Industrial Situations
 - Size
 - Style & Diversity
- Available benchmarks fall far short!

Benchmark Shortcomings



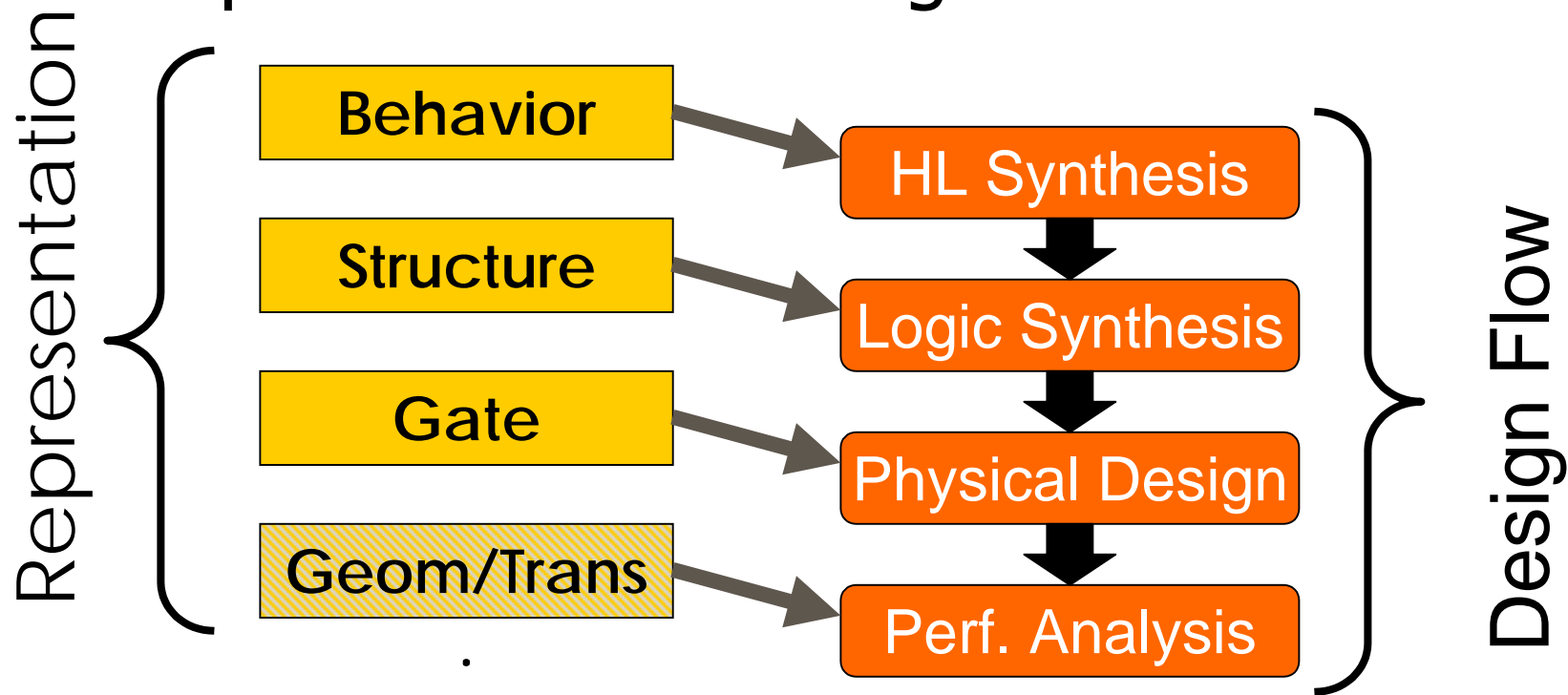
- Too small & questionable diversity
- Non-standard representations
- No system context
 - Does technique improve performance and cost?
- No design-flow context
 - Does technique effect other tools?
- No testing methodology
 - Does technique produce correct designs?

Current Benchmarks

	PREP	ISCAS	LGSynth	HLSynth	CMUDSP
Behavioral				✓	✓
Structural	✓				✓
Gate		✓	✓		✓
Testing	?			Test Vectors	Functional
# Circuits	13	31	202	9	1(3)
Avg. Gates	112	3149	1055	N/A	14550

Vertical Benchmarks

- Multiple representations
- Complete standard design flow



Vertical Benchmarks

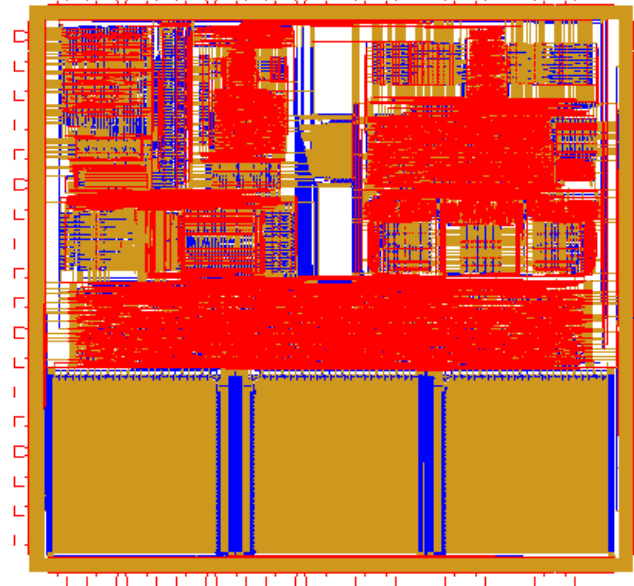


- Useful to many CAD researchers
 - Co-design, Synthesis, Physical Design, Testing ...
- Evaluate CAD in terms of system impacts:
 - Area / Performance
- Evaluate impact on down-stream tools
 - Does fewer gates ⇔ less routability?

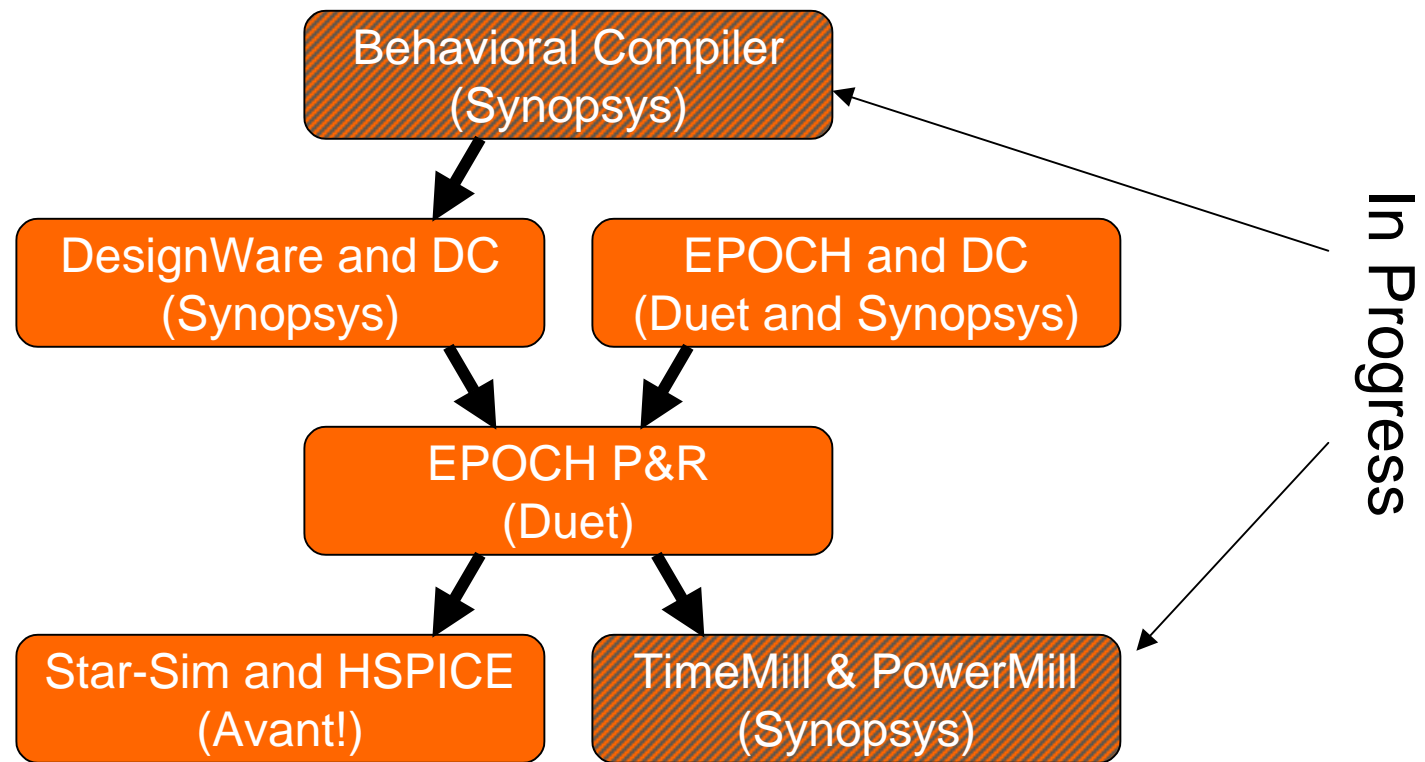
Major Universities have commercial tools

A Vertical Benchmark: CMUDSP

- Based on commercial DSP architecture
- 4x larger than any of listed benchmarks
- Fabricated in $0.5\mu\text{m}$ (30MHz)
- Diversity:
 - Memories
 - Control
 - Data path



Design Flow and Representations



Representations:
Verilog

Testing Methodology



- Program kernels:
 - FFT, FIR, LMS
 - Set memory initial state, run, test final state
 - Scripts to run Verilog, generate SPICE vectors

- Develop different kernels
 - Use commercial compiler/assembler
 - Binary-to-binary translator

CAD Uses Now @ CMU



- Low power circuit/system design
- Synthesis:
 - Application-specific processor design
- Testability, ATPG
- Manufacturability
- Formal Verification
- Cross-disciplinary interaction!

Other Potential Uses



- Behavioral Synthesis
 - Behavior specifies ISA
 - Structural is hand-designed, structured
- Physical design
- Timing analysis
- Circuit design and synthesis
- Design re-use, core-based design

Availability



- Alpha version available now:

<http://www.ece.cmu.edu/research/lowpower>

- Feedback:

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- Version 1.0: December

What Remains to be Done?



- Timing specs for modules
- Improve testing coverage
 - Cover all instruction opcodes
- Complete behavioral specification
- Design using Public Domain Library
- Use Industry-standard P&R tool
 - Silicon Ensemble

New Vertical Benchmarks



- ARM-derived micro-controller
 - Designed, not thoroughly tested
- IDEA encryption ASIC (class project)
- Collaboration?