Vertical Benchmarks and the CMUDSP

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CAD Benchmarks

- Good research requires good benchmarks

- CAD Benchmarks ≈ Industrial Situations
  - Size
  - Style & Diversity

- Available benchmarks fall far short!
Benchmark Shortcomings

- Too small & questionable diversity
- Non-standard representations
- No system context
  - Does technique improve performance and cost?
- No design-flow context
  - Does technique effect other tools?
- No testing methodology
  - Does technique produce correct designs?
# Current Benchmarks

<table>
<thead>
<tr>
<th></th>
<th>PREP</th>
<th>ISCAS</th>
<th>LGSynth</th>
<th>HLSynth</th>
<th>CMUDSP</th>
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<tbody>
<tr>
<td>Behavioral</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Structural</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
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<td>✓</td>
</tr>
<tr>
<td>Gate</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>Testing</td>
<td>?</td>
<td>✓</td>
<td>✓</td>
<td>Test Vectors</td>
<td>Functional</td>
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<td>1055</td>
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Vertical Benchmarks

- Multiple representations
- Complete standard design flow

**Representation**

- **Behavior**
- **Structure**
- **Gate**
- **Geom/Trans**

**Design Flow**

- HL Synthesis
- Logic Synthesis
- Physical Design
- Perf. Analysis
Vertical Benchmarks

- Useful to many CAD researchers
  Co-design, Synthesis, Physical Design, Testing ...
- Evaluate CAD in terms of system impacts:
  Area / Performance
- Evaluate impact on down-stream tools
  Does fewer gates $\Rightarrow$ less routability?

Major Universities have commercial tools
A Vertical Benchmark: CMUDSP

- Based on commercial DSP architecture
- 4x larger than any of listed benchmarks
- Fabricated in 0.5μm (30MHz)

Diversity:
- Memories
- Control
- Data path
Design Flow and Representations

Behavioral Compiler (Synopsys)

- DesignWare and DC (Synopsys)
- EPOCH and DC (Duet and Synopsys)

EPOCH P&R (Duet)

- Star-Sim and HSPICE (Avant!)
- TimeMill & PowerMill (Synopsys)

Representations: Verilog

In Progress
Testing Methodology

- Program kernels:
  - FFT, FIR, LMS
  - Set memory initial state, run, test final state
  - Scripts to run Verilog, generate SPICE vectors

- Develop different kernels
  - Use commercial compiler/assembler
  - Binary-to-binary translator
CAD Uses Now @ CMU

- Low power circuit/system design
- Synthesis:
  - Application-specific processor design
- Testability, ATPG
- Manufacturability
- Formal Verification
- Cross-disciplinary interaction!
Other Potential Uses

- Behavioral Synthesis
  - Behavior specifies ISA
  - Structural is hand-designed, structured
- Physical design
- Timing analysis
- Circuit design and synthesis
- Design re-use, core-based design
Availability

- Alpha version available now:
  http://www.ece.cmu.edu/research/lowpower

- Feedback:
  herman@ece.cmu.edu
  inacio@ece.cmu.edu

- Version 1.0: December
What Remains to be Done?

- Timing specs for modules
- Improve testing coverage
  
  Cover all instruction opcodes

- Complete behavioral specification

- Design using Public Domain Library
- Use Industry-standard P&R tool
  
  Silicon Ensemble
New Vertical Benchmarks

- ARM-derived micro-controller
  - Designed, not thoroughly tested

- IDEA encryption ASIC (class project)

- Collaboration?