Accellera HDL+ Committee:

1. Verilog++ Committee.
2. Assertion Committee
1) **Committee Name And Goals (HDL+).**
HDL+ is focused on extending HDL languages to high level of abstraction combined with assertion verification technology. It contains two committees with the following goals:

a) **Verilog++ Committee:** Extend Verilog 2001 to support architectural and behavioral design (synthesis and verification). The extension is based on Superlog extended synthesis subset (donated by Co-Design) and assertions donations by Verplex.
   i) Deliverables will be an Accellera standard for Verilog++ LRM. This is an extension for IEEE Verilog 2001 standard LRM.
   ii) An updated version will be eventually submitted to IEEE for a possible standardization of Verilog 2005.

b) **Assertion Committee:** Develop Assertions standards for Verilog, VHDL and Accellera C/C++. It provides manual and open source for Verilog library support, with extensions to VHDL and C/C++. The open source will use Source Forge facilities. Assertions are semi-formal monitor / checkers to be used by both simulation and formal tools.
   i) Deliverables will be:
      2) Syntax development for Verilog++ LRM.
      3) Reference implementation as Verilog models first.
      4) Coordination with Accellera Formal Committee (VFV) to ensure Formal Language will follow agreed upon semantics.

2) **Committee members:**
   a) **Verilog++:**
      i) Chair: Vassilios Gerousis (Temporary) Vassilios.Gerousis@Infineon.Com
      ii) and Co-chair: David Kelf (Temporary) davek@co-design.com
   b) **Assertion:**
      i) Chair: John Emmitt johne@verplex.com
      ii) Co-Chair: Harry Foster foster@hp.com

3) **Verilog++ Members**
   Vassilios Gerousis - Infineon
   Harry Foster - Hewlett Packard
   Lauro Rizatti - Get2Chip
   David Knapp - Get2Chip

June 15, 2001
Pradeep Fernandes - Get2Chip  
Dave Kelf - Co-Design  
Phil Moorby - Co-Design  
Simon Davidmann - Co-Design  
Mike McNamara - Verisity Design, IEEE 1364  
John Sanguinetti - Forte design  
Dave Springer - Cynapps  
John Emmitt - Verplex  
KC Cheng – Verplex  
Stu Sutherland - Sutherland HDL, IEEE 1364  
Muraoka – STARC  
David Smith – Avanti! Corporation  
Clifford Cummings – Sunburst Design, IEEE 1364

4) Assertion Members
   John Emmitt ==> Chairman (Verplex)  
   Harry Foster ==> Co-chairman (Hewlett-Packard)  
   Frank Dresig -- AMD  
   Susan Wong -- Axis  
   Jeff Shaffer -- Compaq  
   Sean Dart -- Chronology  
   Steve Dean -- Chronology  
   Mike Meredith -- Chronology  
   Dave Kelf -- Co-Design  
   Henry Cox -- Co-Design  
   Brett Cline -- CynApps  
   Andrew Goodrich – CynApps  
   Jerry Vauk – Sun Micro Systems  
   Claudionor Coelho -- Verplex  
   Michal Siwinski -- Verplex

5) Milestones
   b) January 2002 -- Technical Review Complete
   c) HDLCON 2002 (March 11-12) -- Tutorial and LRM draft.
   d) May 2002: Final draft to Accellera Board and Members
   e) DAC 2002. (June 2002) -- Accellera standard release

6) Donations and Technology Assignment to Accellera
a) Co-Design has donated Superlog Synthesizable subset as the main core for Verilog++. The HDL+ committee reviewed language on June 14.
b) Verplex has donated the assertion library and manual. More members are signing in to participate. Our plans are:
c) Technology assignment to Accellera by both companies were signed and accepted by Accellera.

7) **Deliverables**
   c) Sources models for both Verilog++ and Assertion.

8) **Technical Editor**
   Stu Sutherland.

9) **Publication:**
      i) Email Reflector Is [vlog-pp@eda.org](mailto:vlog-pp@eda.org)
      i) Email Reflector is [assertion@eda.org](mailto:assertion@eda.org)
   d) Manual of OVL (assertion) and Verilog libraries. [http://www.verificationlib.org](http://www.verificationlib.org)

10) **Partnership with Other Organization.**
    Participation by STARC from Japan.