

Desirable features for Standard Accellera Property Specification Language

Clocking

Single clock

1. construct to clearly specify a clock with a clocking boolean expression
2. construct to specify a regular or formula expression under a clock
3. ability to group expressions(regular and formula expressions) for a clock
4. ability to specify one or more clocks
5. ability to default the clock to simulation clock for asynchronous behavior during simulation
6. weak and strong constructs to specify clocks

Multiple clocks

1. ability to synchronize two regular expressions under the same clock
2. ability to synchronize two regular expressions under two different clocks
3. ability to conveniently use multiple clocks in a single formula expression

Expression Definitions

1. construct to define parameterized expressions(boolean, regular and formula)
2. construct to instantiate expression definitions with parameters to bind to different design objects
3. ability to instantiate expression definitions as sub-expressions within another expression
4. ability to associate a clock with the expression definition(regular and formula)

Reset functionality

1. construct to specify a boolean expression as a reset expression
2. construct to specify rejecting a formula as false based on an asynchronous reset expression becoming true
3. construct to specify accepting a formula as true based on an asynchronous reset expression becoming true
4. ability to specify synchronous resets

Verilog Compatibility

Boolean Expressions

1. Verilog compatible boolean operators in syntax and semantics
2. Verilog compatible 4-state evaluation of boolean operators
3. minimize keyword clash with Verilog keywords
4. Verilog conventions for referencing constant expressions

Binding to Design Objects

1. Verilog naming conventions for referencing design objects

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2. Verilog notion of design hierarchy and instantiation of modules
3. ease of use in grouping assertions for a particular instance or a module that defines a design

Macro Expansion

1. Verilog compatible parameterized macro definition capability
2. construct to group assertions and expressions in a parameterized template
3. ability to instantiate templates for binding to specific objects
4. Verilog compatible conditional compilation directives

Regular Expressions

Sequencing

1. intuitive syntax for specifying concatenation and repetition
2. construct to specify a range of repetition from 0 to any number
3. operators to perform union, intersection and some form of negation
4. construct to specify conditional matching
5. constructs to specify properties to hold during a match, such as length and boolean expressions

Timing

1. construct to specify 0 to any number of gap (in terms of clock ticks) between regular expressions
2. operators to specify a range of gap between regular expressions

Specifying Assertions

1. construct to specify expressions (formula, regular and boolean) as assertions
2. construct to construct group of assertions and expressions in a parameterized template
3. construct to instantiate templates for binding to specific objects

Semantic Requirements

1. formal semantics must be specified for the language
2. semantics of any construct should be independent of its context