

# **Accelera Technical Committee**

## **Prepared By Chairs Of TSC**

**Version 1.3, 2Q2001**

**TC Chairman**  
**Vassilios Gerousis**

## Architectural Language Committee

### 1) **Committee Name.**

Architectural Language Committee (ALC). **THE ALC COMMITTEE AND SLDL IS FORMALLY JOINED UNDER ACCLERA TO FOCUS ON SYSTEM LEVEL DESIGN. THE NEW COMBINED COMMITTEE IS CALLED SYSTEM LEVEL DESIGN STANDARDS.**

It has one subcommittee to address C/C++

### 2) **Committee members:**

#### a) Chairs:

- i) Chair: Vassilios Gerousis, Infineon Technologies,  
[Vassilios.Gerousis@Infineon.Com](mailto:Vassilios.Gerousis@Infineon.Com)
- ii) Co-chair: Martin Baynes – Inactive Status

### 3) **Member names** (individual with company affiliation).

#### a) **Active Members**

Martin Baynes C-Level  
 Grant Martin Cadence  
 David Springer CynApps  
 John Sanguinetti CynApps  
 Brian Baley Mentor Graphics.  
 Yaron Kashai Verisity  
 Simon Davidmann Co-Design  
 Dennis Brophy Model Technology  
 Chris Lennard Cadence and VSIA

#### **Other members**

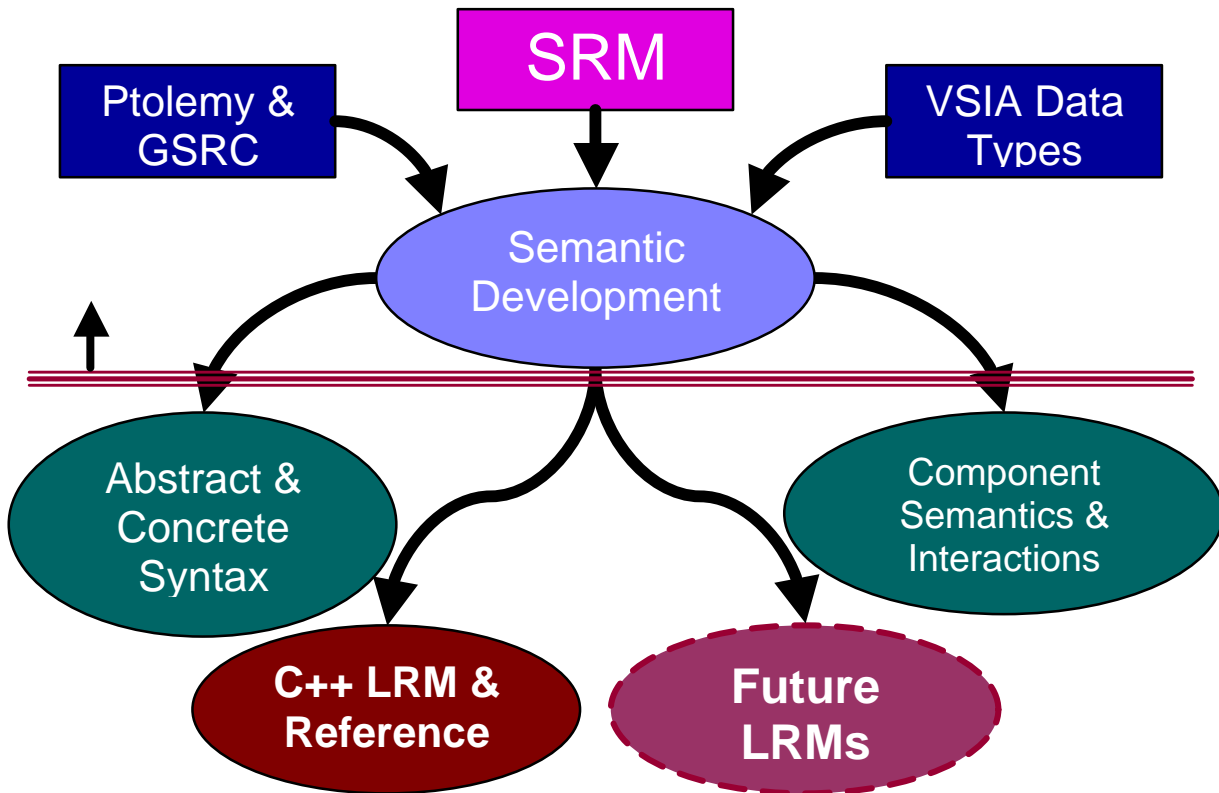
Get2Chip  
 National Semiconductor  
 Motorola  
 Virtio  
 Improv System

### 4) **Goals for the committee** (short term and long term).

#### **(1) ALC Charter**

- Develop an architectural / algorithmic language **Semantics** and **Syntax** standard with verification, analysis, and synthesis orientation.

- SRM will be based on Ptolemy Component Syntax and General Semantics. An agreement with Edward Lee to help on this effort.



- C++ Sub-Group: Language Syntax with reference implementation will be developed first using C++. Additional information can be found below.

#### 5) Schedules And Timelines:

Goal to produce SRM with at least one example appendix early in 2001 for review.

#### 6) Status, issues and Progress.

##### Current Activities

- ★ A complete outline is developed for the SRM. Volunteers for each chapter were established.
- ★ The SRM is based on existing technology from:
  - GSRC concepts for describing architectures.
  - MoML to express concrete syntax in a company independent way.
  - Ptolemy II Models of Computation (MOC) description.

- VSIA taxonomy of terms.

We have established good partnership with Berkeley/GSRC.

## 7) Budget needs

(Technical writing in hours, start time, peak time and possible date for completion).

Technical editing is planned for the beginning of December. The expectation is two hours per week. Peak value of 4 hours per week is expected in February of 2001.

## 8) Publication:

- a- Web Address. <http://www.eda.org/alc-cwg>
- b- Paper.
- c- Tutorial.
- d- Minutes. <http://www.eda.org/alc-cwg/minutes.htm>
- e- Press release :
- f- Conference Communication :
- g- etc..

## 9) Partnership With Other Organization.

ALC has established working relationship with several organizations. VSIA SLD working group and ALC formed a partnership to have Accelera as an umbrella to unify several activities in the System Level Design activities. The organizations are listed below:

- VSIA SLD: We are adopting their data types specification and taxonomy.
- Berkeley Ptolemy/GSRC: We are adopting Ptolemy Semantics and model of computation. We are guided by Professor Ed Lee of UC Berkeley.
- VI SLDL: We started discussions to unify SLDL and ALC under the umbrella of Accelera. The team leaders of SLDL are considering the unification proposal.
- SystemC: I have started the discussion with the members of SystemC to consider alliance in the Semantic definition with Accelera. As stated below SystemC is being represented in the ALC C/C++ working group.
- SpecC: Discussion with SpecC organization has helped in the formation of ALC C/C++.

## 10)References

- ALC C/C++ Language Committee: <http://www.eda.org/alc-wg>
- The Gigascale Silicon Research Center (GSRC) Web Page: <http://www.gigascale.org/>
- Ptolemy II Web Page: <http://ptolemy.eecs.berkeley.edu/ptolemyII/index.htm>

➤ VSIA Web Page : <http://www.vsia.com/>

## ALC C/C++ Sub-Committee

### 1- Committee Name (ALC-CWG).

C/C++ Class Library Standardization Working Group  
This working group is a sub-committee of the ALC

### 2- Committee members:

a- Chair Brian Bailey Mentor Graphics Corp [brian\\_bailey@mentor.com](mailto:brian_bailey@mentor.com)  
and Co-chair Dan Gajski University of California Irvine [gajski@ics.uci.edu](mailto:gajski@ics.uci.edu) names.  
b- Member names (individual with company affiliation).

#### Active Members

Yuri Panchul	C Level Design
Grant Martin	Cadence
Simon Davidmann	CoDesign Automation
Paula Menzigian	Coware
John Sanguinetti, David Springer	CynApps
Duncan Gurley	Fujitsu WWSLT
Kamal Hasmi	ICL
Vassilios Gerousis	Infineon
Asa Ben-Tzur	Intel Corp
Brian Bailey, Dennis Brophy	Mentor Graphics
Shrenik Mehta, Charles Cheng	Sun Microsystems
Kevin Kranen	Synopsys
Daniel Gajski	UC Irvine
Sampath Dakshinamurthy	U & I Scotty Computers Ltd
Filip Thoen	Virtio

#### Other members

Chris Lennard	Cadence
Joe Daniels	Intrinsix

#### Inactive member

Martin Baynes

### 3- Goals for the committee (short term and long term).

The Accellera Architectural Language Committee (ALC) is creating a framework for a Semantic Reference manual (SRM) that will be capable of supporting a number of

models of computation. The SRM requires that these models of computation are defined and an example implementation provided by sub-groups of the ALC. This group, the C/C++ working group has been chartered with the creation of one or more semantic models plus a reference implementation for these using C/C++. Other sub-groups may be formed to look at other domains of computation or concrete syntaxes.

For any semantic model that is defined, the group needs to provide three deliverables.

- First: a definition of the semantics. These semantics must be compatible with the SRM and in a form acceptable to the ALC.
- Second: a concrete syntax for those semantics will be provided using the C/C++ language
- Third: a reference implementation that demonstrates the first two items will be provided in a form that enables wide dissemination of the work.

The eventual goal of the committee is that all of these deliverables will be offered to the IEEE, ISO or other suitable body for standardization. In the shorter timeframe we intend to address the RTL level with the creation of a set of semantics that are useable by both synthesis and verification.

#### 4- Schedules And Timelines:

The group has not defined a formal schedule at this time. We were formed during DAC 2000 with the first meeting held June 27<sup>th</sup>. We have set a short term goal of having an RTL set of semantics defined and demonstrated by the end of the year.

#### 5- **Status, issues and Progress.**

A draft of the RTL semantics is complete and currently going through internal review. Within the next few weeks it will be sent out to a larger audience for comments before final stage formatting. In addition, we are currently constructing a condensed semantic reference guide that will go in as an appendix to the manual. We are currently planning activities for the next stage of this work, which will take us up to higher levels of abstraction. We need to formulate a rollout schedule for release and publicity associated with it.

#### 6- **Budget needs**

We are in need of writing resources immediately. We have a completed draft document on which we have almost settled all technical content. We now need to prepare it for formal release.

#### 7- **Publication:**

- a- Web Address. <http://www.eda.org/alc-cwg>
- b- Paper.

- c- Tutorial.
- d- Minutes. <http://www.eda.org/alc-cwg/minutes.htm>
- e- Press release :
- f- Conference Communication :
- g- etc..

#### 8- **Partnership With Other Organization.**

We have informal relationships with 3 organization.

- VSIA. We are adopting their data types specification and taxonomy.
- SystemC. We have an asynchronous communication with this organization plus representation in the committee.
- SpecC. We have contacted them regarding closer working relationship which will become more established in the second phase of this program when we address higher levels of abstraction.

## Advanced Library Format (ALF)

### 1) **Committee Name.**

Advanced Library Format Workgroup

### 2) **Committee members:**

#### a- Chairs:

- **Chair:** Wolfgang Roethig, NEC Electronics, [Wolfgang\\_Roethig@el.nec.com](mailto:Wolfgang_Roethig@el.nec.com)
- **Co-chair** Mike Andrews, Mentor Graphics, [Mike\\_Andrews@mentor.com](mailto:Mike_Andrews@mentor.com)

#### b- Member names (individual with company affiliation).

#### **Function, Synthesis, DFT, Electrical Performance modeling subgroup**

Tim Ayres,	Synopsys
Arun Balakrishnan,	NEC Electronics
Shir-Shen Chang,	Synopsys
Gregory duFour,	Mentor Graphics
Tim Ehrler,	Philips
Pierre Girouard,	Logicvision
Tim Jennings,	Philips
Stephen Pateras,	Logicvision
John Peters,	Philips
Sergei Sokolov,	Sequence
Gopal Varshney,	Philips

#### **Physical layout modeling subgroup (formerly OPEF)**

Tom Belpasso,	Cadence
Simon Favre,	Monterey Design Systems
Joe Morrell,	IBM
Anand Sethurami,	LSI Logic
Paul Zukowski,	IBM

#### **Links-to-OLA subgroup**

Jay Abraham,	Silicon Metrics
John Beatty,	IBM
Dan Moritz,	LSI Logic
Dhaval Sejpal,	IBM

More than 50 members on the email reflector [alf@eda.org](mailto:alf@eda.org)

The members listed here have contributed to the ALF 2.0 specification. The members committed to support the IEEE study group will be reported by March 2.

### **3) Goals for the committee (short term and long term).**

The goal of ALF is to develop a comprehensive description of functional, electrical and physical models for cells and building blocks in SOC designs. In addition to synthesis-and DFT-oriented function, timing, and power description, ALF provides also state of the art modeling capabilities for noise, electromigration and physical layout rules in VDSM design. More detailed goals can be viewed at the ALF webpage (<http://www.eda.org/alf>).

The ALF committee has also developed a proposal for a common ALF/OLA roadmap, published on the same webpage.

### **4) Schedules and timelines**

ALF 2.0 has been approved as Accellera standard in November 2000. The previous version ALF 1.1 has been approved as OVI standard in April 1999.

ALF IEEE study group is to be formed and recognized by DASC in Q1 2001.

Tentative schedule:

- IEEE study group: Q1 2001 - Q3 2001.
- Transformation into IEEE work group: Q4 2001.
- Development of IEEE draft document: Q4 2001 – Q1 2002.
- Review and ballot: Q2 2002 – Q3 2002.
- Eventual 2<sup>nd</sup> round of review and ballot: Q4 2002.

### **5) Status, issues and progress**

ALF 2.0 LRM and tutorial are available on <http://www.eda.org/alf>.

The ALF workgroup is now in a transition phase between Accellera workgroup and IEEE study group. An informal meeting on the ALF strategy has been held between Accellera chair Dennis Brophy, Vice-chair Steve Schultz and ALF workgroup chair Wolfgang Roethig at ASP-DAC 2001.

Preparation for IEEE is on schedule: Kickoff meeting for IEEE scheduled for February 20, DASC meeting on February 28.

Need to secure the following resources:

- Technical editor (propose to continue the contract with Joe Daniels)
- Webpage administrator (currently done by Mike Andrews, who is pretty overloaded)

Need Accellera marketing strategy for ALF. Proposed approach by Dennis Brophy and Steve Schultz: focus on library data model for next-generation design tools.

To our knowledge, 3 commercial EDA tool vendors, 2 commercial library vendors, 3 or more silicon vendors support ALF 1.1 today. We have commitment from 2 EDA tool vendors and at least 1 silicon vendor to support ALF 2.0 by e/o 2001. This information has been obtained through internal communication channels. Accellera should establish a system to monitor, verify and report the evolution of ALF support on a regular basis.

Accellera should push for open-source sample libraries as well as open-source ALF parsers from the supporting companies in order to create a self-sustaining ALF test lab.

#### 6) **Budget needs**

Pending on resource allocation decision.

#### 7) **Publication:**

a- Web Address. <http://www.eda.org/alf>

b- Paper:

- "On-chip power evaluation methods and solutions" HP Design conference 1997
- "A new modeling approach for unified power and timing characterization for ASIC libraries" Poster session, DATE 1998.
- "Signal integrity on SOC" Plenary session ASIC SOC conference 2000 (staged on <http://www.necel.com>)

c- Tutorial.

- HDL conference 1998
- HDL conference 2000 (staged on <http://www.eda.org/alf>)

d- Minutes: <http://www.eda.org/alf>

e- Press release : ALF committee has put together a press release which is now handled by Dennis Brophy.

f- Conference Communication:

- ALF tutorial and panel on CICC 2001.
- Other opportunities:
- ISPD 2001 (panel organized by SUN, pending)
- DAC 2001 (panel organized by Sequence, pending)

#### **Partnership With Other Organization.**

We have an informal relationship with the OLA workgroup sponsored by Si2. This relation as well as eventual relations to other organizations are subject to re-assessment by the IEEE study group.



## Formal Verification

### 1) Committee Name.

Formal Verification Committee. ([www.eda.org/vfv](http://www.eda.org/vfv))

### 2) Committee members:

#### 1- Chairs:

- a- Chair: Harry Foster, HP, [foster@rsn.hp.com](mailto:foster@rsn.hp.com)
- b- Co-chair: Carl Pixley, Motorola, [pixley@adtx.sps.mot.com](mailto:pixley@adtx.sps.mot.com)

#### 2- Member names (individual with company affiliation).

- Arif Samad (Synopsys) <arif@synopsys.com>
- Cindy Eisner (IBM) <eisner@il.ibm.com>
- Claudionor Coelho (Verplex) <coelho@verplex.com>
- Danny Geist (IBM) <Danny\_Geist@il.ibm.com>
- Ed Clarke (CMU) <Edmund.Clarke@cs.cmu.edu>
- Erich Marschner (Cadence) <erichm@cadence.com>
- Ghassan Khoory (Synopsys) <gkhoory@synopsys.com>
- Hillel Miller (Motorola) <hillelm@msil.sps.mot.com>
- J. Bhasker (Cadence) <jbhasker@cadence.com>
- John Zhong <zhong@innologic-systems.com>
- K.C.Chen (Verplex) <kchen@verplex.com>
- Matthew Morley (Verisity) <matthew@verisity.com>
- Mike McNamara (Verisity) <mac@verisity.com>
- Peter Flake (Co-Design) <flake@co-design.com>
- Prakash Narain (Realintent) <prakash@realintent.com>
- Shoham Ben David (IBM) <shoham@il.ibm.com>
- Sudhir Kadkade (Silicon Forest Research) <Sudhir\_Kadkade@sifr.com>
- Surrendra Dudani (Synopsys) <dudani@synopsys.com>
- Tom Anderson (0-in) <tla@0-in.com>
- Tom Fitzpatrick (Cadence) <tfitz@cadence.com>
- Vassilios Gerousis (Infineon) <Vassilios.Gerousis@infineon.com>
- Yaron Kashai (Verisity) <yaron@verisity.com>
- Yaron Wolfstal (IBM) <wolfstal@il.ibm.com>

### 3) Goals for the committee (short term and long term).

#### **GOALS:**

1. To define a standard for design that can be formally verified.
2. To define a standard for properties that are used for proofs and constraints
3. To define output formats from formal verification tools. To define output formats from formal verification tools results coverage counter examples trace any other debug information

#### **Deliverables**

1. Syntax and semantics for formally synthesizable subset of Verilog.
2. Syntax and semantics for verification properties which will can be proved to check functionality of a design or which will constrain the design to work in well defined environment.
3. Syntax and semantics for output formats
4. Some definitions for inter operability of equivalency checking.

#### **The goals for the property description language are:**

The basic goals of the proposed Property Specification Language (PSL) are:

1. *Simplicity* - the PSL must be easy to understand and use by engineers familiar with today's HDLs.
2. *Conciseness* - the PSL semantics must be unambiguous.
3. *Expressiveness* - the PSL must support temporal logic.
4. *Consistency* - the PSL must support an assume guarantee reasoning paradigm, which is to say environmental constraints as well as design properties use the same syntax and semantics.
5. *Generality* - the PSL should be compatible (when possible) across simulations methods as well as formal methods.
6. *Acceptance* - the design community should actively embraces the PSL standard.

#### **Property Description Language Requirements**

- The syntax and semantics shall be described precisely and available for review.
- The language applications shall be available for demonstration and test.
- The language shall support describing constraints and properties in an interchangeable fashion.
- The language shall support multiple clock domains.
- The language shall support safety, liveness and fairness descriptions.
- The language shall support state machine checks such as deadlock, livelock, unreachable states, path and clique properties, and state transition properties.
- The language should support checks for conflicting constraints

- This language should support coverage measures related to states and state-transitions.
- Constraints and properties shall be allowed on internal nodes along with inputs, outputs.
- The *syntax* for the Property Specification Language (PSL) must be precisely defined.
- The *semantics* for the PSL must be precisely defined.
- The language must support an *assume-guarantee reasoning paradigm* with environmental constraints and design properties expressed in an interchangeable fashion.
- The PSL must support both *synchronous* as well as *asynchronous* property specification.
- The PSL must support *invariant* specification.
- The PSL must support *liveness* specification.
- The PSL must define a means for *fairness* specification.
- The PSL must support properties related to variable Z values.
- The PSL must support variable X values.
- The PSL must support expressing branching time logic properties.

DOD can be accessed at <http://www.eda.org/vfv/>.

#### 4) **Schedules And Timelines:**

The Accellera Formal Verification Technical Committee will base its draft property specification language (PSL) standard on a strawman of existing and proven technology. Hence, the following language contributions have been made to Accellera for this purpose:

- *Temporal e* from Verisity Design, Inc.
- *Sugar* from International Business Machines
- *CBV* from Motorola

The committee is actively establishing language contribution acceptance criteria. Each of the three contributions will be judged against this criteria.

The chairman has set a goal to select the strawman based on the 3 contributions by July, 2001. These goals need to be approved by the entire committee.

#### 5) **Status, issues and Progress.**

The committee is undergoing restructuring and will have appropriate reports in time.

#### 6) **Budget needs**

Technical Committee Summary July 19, 2001  
Technical Chairman: Vassilios Gerousis

We will wait for better estimate, when the committee has finalized its plans.

7) **Publication:**

- a- Web Address. <http://www.eda.org/vfv>
- b- Paper:
- c- Tutorial.
- d- Minutes: <http://www.eda.org/vfv/hm>
- e- Press release :
- f- Conference Communication :

8) **Partnership With Other Organization.**

## Verilog-AMS

1) **Committee Name.**

**Verilog-AMS:** Verilog analog and mixed signal language.

2) **Committee members:**

a) Chairs:

- i) Chair: Ian Wilson, Antrim Design Systems
- ii) Co-chair: Kevin Cameron, National Semiconductor

3) **Member names** (individual with company affiliation).

**Active Members**

Ken Bakalar	Mentor Graphics
Sri Chandrasekaran	Motorola
Joe Daniels	Seva
Dan FitzPatrick	Synopsys
Vassilios Gerousis	Infineon
Steve Grout	Tality
Graham Helwig	Motorola
Peter Liebman	Antrim
Steve Meyer	Pragmatic
Ira Miller	Motorola
Martin O'Leary	Cadence
Jon Sanders	Cadence
John Shields	Avanti

**Other members**

4) **Goals for the committee** (short term and long term).

The committee has already delivered three OVI standards. The latest version is Verilog-AMS version 2.0. The plan is to produce one more revision (2.1) of the manual to resolve major issues and ambiguities; this revision will be further updated for 1364-2001 compliance and VPI changes and reworked for IEEE submission.

5) **Schedules And Timelines:**

The 2.1 LRM revision will be made available mid-2001.

Joe Daniels estimates 6-12 months elapsed time to get from this to IEEE level.

**6) Status, issues and Progress.**

Issues will be considered only if they are accompanied by proposed solutions and/or workarounds. Similarly, discussion topics must be accompanied by a position statement or detailed proposal.

Must have all input in process by beginning of March to make mid-year target.

**7) Budget needs**

(Technical writing in hours, start time, peak time and possible date for completion).

200 hours budgeted, primarily for the IEEE rework phase.

**8) Publication:**

a- Web Address. <http://www.eda.org/verilog-ams>

Mailing list [verilog-ams@eda.org](mailto:verilog-ams@eda.org)

b- Paper.

c- Tutorial.

d- Minutes.

e- Press release :

f- Conference Communication :

g- Design Objectives: on web site

h- Examples: on web site

**9) Partnership With Other Organization.**

Discussions with IEEE VHDL-AMS are usually going to ensure compatibility in the next releases. We will pursue this as a formal process.

## Design Constraints (DEFUNCT)

1) **Committee Name.**

Accellera Design Constraints Working Group. <http://www.eda.org/dcwg/>

2) **Committee members:**

a) Chairs:

i) Chair: Mark Hahn, Cadence, [mhahn@cadence.com](mailto:mhahn@cadence.com)

ii) Co-chair:

3) **Member names** (individual with company affiliation).

**Active Members**

Cadence

IBM

Mentor Graphics.

TI

Infineon

VSIA members.

SLDL members

**Other members**

Avanti / Analogy

4) **Goals for the committee** (short term and long term).

The Design Constraints Working Group (DC-WG) is defining a standard called the Design Constraints Description Language (DCDL).

The objective of DCDL is to make it possible for designers to consistently specify, apply, and reuse constraint descriptions in order to describe design intent for EDA tools.

DCDL is a set of commands that express design intent for all constraint domains within each electronic design flow. DCDL provides a syntactical and semantic definition that is language and tool independent. The group created a taxonomy that contains the required set of commands that cover today's timing domain and predicted future needs. This was accomplished by working with designers and EDA vendors. The taxonomy was then mapped to syntax compatible with TCL and the System Level Design

Language (SLDL). Finally, semantic documentation was created for each command and prototype readers were created. Finally, semantic documentation was created for each command and prototype readers were created.

The DC-WG will work through each constraint domain using this method.

5) **Schedules and Timelines:**

A new schedule will be published for the next version.

6) **Status issues and Progress: DEFUNCT**

**THIS COMMITTEE IS DEFUNCT. COMMITTEE CHAIR FROM CADENCE HAS STOPPED DEVELOPMENT DUE:**

**1- LACK OF PARTICIPATION BY MEMBER COMPANIES.**

**2- CADENCE ACCESSES TO SYNOPSYS DESIGN CONSTRAINT THROUGH PRIVATE DISCUSSIONS.**

**3- SYNOPSYS PUTTING SDC IN THE "OPEN SOURCE".**

7) **Budget needs**

(Technical writing in hours starts time, peak time and possible date for completion).

We will wait for the planning process.

8) **Publication:**

a- Web Address. <http://www.eda.org/dcwg>

b- Paper.

c- Tutorial.

d- Minutes.

e- Press release :

➤ ISD Magazine, September 1999

➤ EE Times, June 1999

➤ EE Times, June 1999

➤ Electronic News, May 1999

➤ EE Times, April 1999

➤ OVI press release, April 1999

f- Conference Communication :

➤ DAC '99: Birds of A Feather Session

➤ EDP '99: Sixth IEEE/DATC Electronic Design Processes Workshop Paper

➤ FDL '98: SLDL Workshop

g- etc.

9) **Partnership With Other Organization.**

DCDL has started as a cooperation between OVI and VSIA as a joint team. The team used Cadence donation as well good cooperation from IBM and Mentor to provide excellent consistent semantics.

SLDL joined in last year to help in the system level and timing area, power and good semantics analysis.

## IEEE 1364.1 Verilog Synthesis

1) **Committee Name.**

Verilog Synthesis Interoperability Working Group.

2) **Committee members:**

a) Chairs:

i) Chair: J. Bhasker, Cadence, jbhasker@cadence.com

ii) Co-chair:

3) **Member names** (individual with company affiliation).

**TASK LEADERS**

Pragmas: Doug Smith

Syntax: Don Hejna

Semantics: Ken Coffman

Web admin: David Bishop

Editor: Yatin Trivedi

**Other members**

100 persons on the email reflector

4) **Goals for the committee** (short term and long term).

The Design Constraints Working Group (DC-WG) is defining a standard called the Design Constraints Description Language (DCDL).

The objective of DCDL is to make it possible for designers to consistently specify, apply, and reuse constraint descriptions in order to describe design intent for EDA tools.

To define syntax and (synthesis) semantics, which can be, used in common by all compliant RTL synthesis tools to achieve uniformity of results in a similar manner to which simulation tools use the IEEE 1364 standard.

This is also described on our home page.

**Schedules and Timelines:**

Work was in full swing to define a standard from July 98 to July 99.

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Technical Chairman: Vassilios Gerousis

At that point, some WG members felt that Verilog 2000 was imminent and that it did not make sense to base the standard on Verilog 95.

However, Verilog 2000 has been substantially delayed since then.

A draft version of the standard based on Verilog 95 is available on our web site.

Plan is to get the WG going again once the Verilog 2000 language is balloted and approved.

#### 5) **Status issues and Progress.**

See 4.

- The WG has definitely lost momentum in establishing a standard. Many of the important participants including some of the task leaders have changed companies and may no longer be willing to participate.
- However, once Verilog 2000 is finalized, the chair will need about 3-4 months to regroup the WG, and then about a year to update, the 1.3 draft based on the Verilog 2000 standard.

#### 6) **Budget needs**

(Technical writing in hours starts time, peak time and possible date for completion).

No budget is required at this time. However, once the WG becomes active, the committee will definitely need technical writing help. We anticipate about 4-5 hours a month.

#### **Publication:**

- Web address: <http://www.eda.org/vlog-synth>
- Email reflector: [vlog-synth@eda.org](mailto:vlog-synth@eda.org)

All email of WG is archived at our web site (thanks to David Bishop).

#### 7) **Partnership With Other Organization.**

Since the chairman did a good job at the VHDL synthesis subset, he will ensure interoperability between the two languages.

## IEEE 1497 SDF Working Group

### Committee members:

Ted Elkind	Chair	Cadence Design Systems
Steve Wadsworth	Co-chair	AMI
Naveen Gupta		LSI Logic
John Amoroux		Ikos
Pierrick Pedron		Synopsys / Now at Ifineon
Brien Anderson		Acuson
Chris Browy		Avery Design Systems

### Long term goal

Make SDF an IEEE standard

### Short term goal

Produce package for review by REVCOM

### Schedule

Produce Revcom package - as soon as time is available ?

### Status

SDF passed balloting last year. There was one negative vote requiring a recirculation, which just took place a few weeks ago.

### Web address

<http://www.eda.org/sdf>

## HDL+ Committee

### 1) Committee Name And Goals (HDL+).

HDL+ is focused on extending HDL languages to high level of abstraction combined with assertion verification technology. It contains two committees with the following goals:

- a) **Verilog++ Committee:** Extend Verilog 2001 to support architectural and behavioral design (synthesis and verification). The extension is based on Superlog extended synthesis subset (donated by Co-Design) and assertions donations by Verplex.
  - i) Deliverables will be an Accellera standard for Verilog++ LRM. This is an extension for IEEE Verilog 2001 standard LRM.
  - ii) An updated version will be eventually submitted to IEEE for a possible standardization of Verilog 2005.
- b) **Assertion Committee:** Develop Assertions standards for Verilog, VHDL and Accellera C/C++. It provides manual and open source for Verilog library support, with extensions to VHDL and C/C++. The open source will use Source Forge facilities. Assertions are semi-formal monitor / checkers to be used by both simulation and formal tools.
  - i) Deliverables will be:
    - (1) Assertion SRM: Semantic Reference Manual for assertion primitives and macro extension.
    - (2) Syntax development for Verilog++ LRM.
    - (3) Reference implementation as Verilog models first.
    - (4) Coordination with Accellera Formal Committee (VFV) to ensure Formal Language will follow agreed upon semantics.

### 2) Committee members:

- a) **Verilog++:**
  - i) Chair: Vassilios Gerousis (Temporary) [Vassilios.Gerousis@Infineon.Com](mailto:Vassilios.Gerousis@Infineon.Com)
  - ii) and Co-chair: David Kelf (Temporary) [davek@co-design.com](mailto:davek@co-design.com)
- b) **Assertion:**
  - i) Chair: John Emmitt [johne@verplex.com](mailto:johne@verplex.com)
  - ii) Co-Chair: Harry Foster [foster@hp.com](mailto:foster@hp.com)

### 3) Verilog++ Members

Vassilios Gerousis - Infineon  
Harry Foster - Hewlett Packard  
Lauro Rizatti - Get2Chip  
David Knapp - Get2Chip

Pradeep Fernandes - Get2Chip  
Dave Kelf - Co-Design  
Phil Moorby - Co-Design  
Simon Davidmann - Co-Design  
Mike McNamara - Verisity Design, IEEE 1364  
John Sanguinetti - Forte design  
Dave Springer - Cynapps  
John Emmitt - Verplex  
KC Cheng – Verplex  
Stu Sutherland - Sutherland HDL, IEEE 1364  
Muraoka – STARC  
David Smith – Avanti! Corporation  
Clifford Cummings – Sunburst Design, IEEE 1364

#### 4) Assertion Members

John Emmitt ==> Chairman (Verplex)  
Harry Foster ==> Co-chairman (Hewlett-Packard)  
Frank Dresig -- AMD  
Susan Wong -- Axis  
Jeff Shaffer -- Compaq  
Sean Dart -- Chronology  
Steve Dean -- Chronology  
Mike Meredith -- Chronology  
Dave Kelf -- Co-Design  
Henry Cox -- Co-Design  
Brett Cline -- CynApps  
Andrew Goodrich – CynApps  
Jerry Vauk – Sun Micro Systems  
Claudionor Coelho -- Verplex  
Michal Siwinski -- Verplex

#### 5) Milestones

- a) F/B conference Sept. 23. -- Complete Preliminary technical contents. V2001, V++ tutorial (turn V2001 session into V++).
- b) January 2002 -- Technical Review Complete
- c) HDLCON 2002 (March 11-12) -- Tutorial and LRM draft.
- d) May 2002: Final draft to Accellera Board and Members
- e) DAC 2002. (June 2002) -- Accellera standard release

#### 6) Donations and Technology Assignment to Accellera

- a) Co-Design has donated Superlog Synthesizable subset as the main core for Verilog++. The HDL+ committee reviewed language on June 14.
- b) Verplex has donated the assertion library and manual.  
More members are signing in to participate. Our plans are:
- c) Technology assignment to Accellera by both companies were signed and accepted by Accellera.

#### 7) **Deliverables**

- a) Language Reference Manual for Verilog++.
- b) Semantic Reference Manual for Assertion.
- c) Sources models for both Verilog++ and Assertion.

#### 8) **Technical Editor**

Stu Sutherland.

#### 9) **Publication:**

- a) Web Address <http://www.eda.org/vlog-pp> (Under Construction).
  - i) Email Reflector Is [vlog-pp@eda.org](mailto:vlog-pp@eda.org)
- b) Web Address <http://www.eda.org/assertion> (Under constructions).
  - i) Email Reflector is [assertion@eda.org](mailto:assertion@eda.org)
- c) Tutorial of Verilog++ at DAC 2001.
- d) Manual of OVL (assertion) and Verilog libraries. <http://www.verificationlib.org>

#### 10) **Partnership with Other Organization.**

Participation by STARC from Japan.