Spice Interoperability with VHDL-AMS
Outline

- Problems and requirements
- VHDL-AMS models for Spice devices
- VHDL-AMS interface for tool-integrated components
- Conclusion and further direction
Compatibility Problems

- Spice is not a single language but rather a family of related languages

- Modification of the language standard (Berkeley) and of the device parameters by many EDA vendors

- A great deal of incompatibility among the Spice language dialects
  - Names of built-in primitives (can) differ
  - Names of parameters (can) differ
  - Names of ports (can) differ

- Different Spice language dialects should be supported
Some Requirements in Device Modeling

- Handling of model parameters
  - Defined on a .model card in Spice

- Model initialization
  - Parameter defaulting and range checking

- Handling of instance parameters
  - Defined on device instance

- Instance initialization
  - Parameter defaulting and range checking

- Interaction with Simulator Variables/Algorithms

Problems and Requirements

Special Problems

- VHDL-AMS models for Spice devices (primitives)
- VHDL-AMS interface for tool-integrated
  - Spice subcircuits
  - Spice primitives
- Identification of terminals (nodes) of VHDL-AMS and Spice models
- Handling of tool-integrated models in other languages
## Library SPICE2VHD

### Entities

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<tr>
<th>Entity</th>
<th>Description</th>
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<td>BJT</td>
<td>Spice Bipolar Junction Transistor (NPN/PNP)</td>
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<tr>
<td>BJT_TH</td>
<td>Spice Bipolar Junction Transistor with thermal terminal (NPN/PNP)</td>
</tr>
<tr>
<td>G8AVTTR</td>
<td>Spice Capacitor Model</td>
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<td>Spice P-N Current Controlled Switch Model</td>
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<tr>
<td>PN1EN</td>
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<tr>
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<tr>
<td>SR1FT</td>
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<tr>
<td>SR1SE</td>
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<td>SR1N1</td>
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<tr>
<td>SR1NS</td>
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<tr>
<td>SR1FT</td>
<td>Spice Junction Field-Effect Transistor (JFET, F)</td>
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<tr>
<td>SR1FT TH</td>
<td>Spice Junction Field-Effect Transistor (JFET, F) with thermal terminal</td>
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<td>MNFET</td>
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<td>MNFET激励</td>
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<td>RESISTOR_CAPACITOR</td>
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<td>RESISTOR_RESISTOR</td>
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<td>VN1</td>
<td>Spice Voltage Controlled Switch Model</td>
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<td>TH1</td>
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<td>TH1UN</td>
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### Package SPICE_PARAMETERS with functions for
- Model initialization and range checking
- Parameter defaulting and

### Spice-like models in VHDL-AMS
- Parameter defaulting
- Port names
- Identifiers in accordance with Spice3F5
- Currently only Level 1 models

Example

Spice netlist

```spice
.MODEL VERTNPN NPN BF=80 IS=1E-18 RB=100 VAF=50
+ CJB=3PF CJC=2PF CJS=2PF TF=0.3NS TR=6NS

.SUBCKT diffPair c1 b1 e c2 b2
Q1 c1 b1 e vertNPN
Q2 c2 b2 e vertNPN
.ENDS
```
… cont‘d Example – VHDL-AMS (1)

library IEEE, SPICE2VHD;
use IEEE.ELECTRICAL_SYSTEMS.all;
use SPICE2VHD.SPICE_PARAMETERS.all;

entity diffPair is
  port (  
    terminal C1, B1, E, C2, B2 : ELECTRICAL
  );
end entity diffPair;
... cont’d Example - VHDL-AMS (2)

architecture a0 of diffPair is

constant vertNPN : BJT_DATA := SET_BJT_DATA (  
  MODEL => NPN,    BF  => 80.0,  
  ISS  => 1.0E-18,  RB  => 100.0,  
  VAF => 50.0,    CJE => 3.0E-12,  
  CJC => 2.0E-12,  CJS => 2.0E-12,  
  TF  => 0.3E-9,   TR  => 6.0E-9);

begin
  Q1: entity BJT(SPICE)  
      generic map (vertNPN)  
      port map (c1, b1, e);
  Q2: entity BJT(SPICE)  
      generic map (MDATA => vertNPN)  
      port map (NC => c2, NB => b2,  
                 NE => e);

end architecture a0;
Package SPICE_PARAMETERS (1)

- Types for declaration of constants with model card data
  - RESISTOR_DATA
  - DIODE_DATA
  - BJT_DATA
  - ...

- Functions to initialize constants with model data
  - SET_RESISTOR_DATA
  - SET_DIODE_DATA
  - SET_BJT_DATA
  - ...

VHDL-AMS models for Spice devices
Package SPICE_PARAMETERS (2)

type MODEL_TYPE is (
  UNDEF, -- model type is not defined
  R, -- semiconductor resistor model
  C, -- semiconductor capacitor model
  SW, -- voltage controlled switch
  CSW, -- current controlled switch
  URC, -- uniform distributed rc model
  LTRA, -- lossy transmission line model
  D, -- diode model
  NPN, -- npn BJT model
  PNP, -- pnp BJT model
  NJF, -- n-channel JFET model
  PJF, -- p-channel JFET model
  NMOS, -- n-channel MOSFET model
  PMOS, -- p-channel MOSFET model
  NMF, -- n-channel MESFET model
  PMF -- p-channel MESFET model
);

Type declaration corresponds to different .model cards

.model vertnpn NPN ...
Package SPICE_PARAMETERS (3)

```vhdl
package SPICE_PARAMETERS is

  type BJT_DATA is array (NATURAL) of REAL;  -- implementation dependent

  function SET_BJT_DATA (  
    constant MODEL   : MODEL_TYPE;        -- type of BJT (NPN|PNP)  
    constant ISS    : REAL := 1.0E-16;   -- saturation current (in A)  
    constant BF     : REAL := 100.0;     -- ideal maximum forward BETA  
    constant NF     : REAL := 1.0;       -- forward current emission coeff.  
    constant VAF    : REAL := REAL'HIGH; -- forward Early voltage (in V)  
    ...  
  ) return BJT_DATA;

end package SPICE_PARAMETERS;
```

Initialization of VHDL-AMS models w.r.t. Spice3f5
Declaration of an entity Declaration

entity BJT is

    generic ( MDATA : BJT_DATA ;
               AREA : REAL := 1.0;
               START : START_TYPE := UNDEF;
               IC_VBE : REAL := REAL'LOW;
               IC_VCE : REAL := REAL'LOW;
               TEMP : REAL := SPICE_TEMPERATURE );

    port ( terminal NC : ELECTRICAL;
               terminal NB : ELECTRICAL;
               terminal NE : ELECTRICAL );

    begin

    assert AREA >= 1.0
    report "AREA >= 1.0 required." severity error;

    assert START = UNDEF or START = IC_OFF
    report "START must be UNDEF or IC_OFF" severity error;

end entity BJT;

Handling of optional terminals not quite clear
(see bulk connection)
Special Arrangements

- No access to simulator variables/algorithms
  - TSTEP => 0.0 or 1.0E-15
  - TSTOP => REAL‘HIGH
  - 1/TSTOP => 0.0
  - Infinite => REAL‘HIGH
  - TEMP => AMBIENT_TEMPERATURE from Package MATERIAL_CONSTANTS

- Handling of model and instance parameter
  - Default value => can be overwritten
  - No default value => value assignment required
  - Detect specification => default to UNDEF
    (REAL‘LOW if parameter is REAL)
Spice Models in SPICE2VHD

- Basic elements
  - RESISTOR, SEMICONDUCTOR_RESISTOR
  - CAPACITOR, INDUCTOR
- Controlled sources and lossless line
  - VCVS, VCCS, TLINE
- Independent voltage sources
  - VDC, VEXP, VPULSE, VPWL, VSINE, VSFFM
- Independent current sources
  - IDC, IEXP, IPULSE, IPWL, ISINE, ISFFM
- Device models
  - DIODE, BJT, MOSFET
Parameterized Models in SPICE2VHD_DEVICES

entity BJT_NPN is

generic
(
  AREA : REAL       := 1.0;
  START : START_TYPE := UNDEF;
  IC_VBE : REAL       := REAL'LOW;
  IC_VCE : REAL       := REAL'LOW;
  TEMP : REAL       := SPICE_TEMPERATURE );

port
(
  terminal NC : ELECTRICAL;
  terminal NB : ELECTRICAL;
  terminal NE : ELECTRICAL );

end entity BJT_NPN;

architecture QNL of BJT_NPN is

constant MODEL_CARD: BJT_DATA:= SET_BJT_DATA(
  MODEL => NPN,
  BF => 80.0,
  RB => 100.0,
  TF => 0.3E-9,
  TR => 6.0E-9,
  CJE => 3.0E-12,
  CJC => 2.0E-12);

begin

T1: entity SPICE2VHD.BJT(SPICE)

generic map ( MDATA => MODEL_CARD,
  AREA => AREA,
  START => START,
  IC_VBE => IC_VBE,
  IC_VCE => IC_VCE,
  TEMP => TEMP);

port map ( NC => NC,
  NB => NB,
  NE => NE );

end architecture QNL;

Entity identifier informs about primitive

Architecture identifier informs about used model card

See: http://fat-ak30.eas.iis.fraunhofer.de/vdalibs/doc
Interface to Spice Subcircuits

- Different solutions to instantiate Spice subcircuits from VHDL-AMS simulators

- Difficulties to exchange models

- What is needed
  - Standard how to „instantiate“ Spice subcircuits
  - Two problems
    - Declaration of the interface in VHDL-AMS
    - Mapping between Spice interface terminals and parameters and VHDL-AMS terminal ports and generic parameters resp.
Interface to Spice Primitives

- As known, no solution to instantiate Spice primitives in VHDL-AMS simulators
- „Work arounds“ using „subcircuit wrappers for primitives“
- Difficulties to exchange models

What is needed

- Standard how to „instantiate“ Spice primitives
- Problems
  - Declaration of the interface in VHDL-AMS
  - Mapping between Spice interface terminals and parameters and VHDL-AMS terminal ports and generic parameters resp.
  - Handling of .modelcards
Global nodes

- Global nodes can be declared in VHDL-AMS in a package

- Example

  ```vhdl
  package GLOBAL_NODES is
    terminal VDD : ELECTRICAL;
    terminal VSS : ELECTRICAL;
  end package GLOBAL_NODES;
  ```

- Different solutions to map Spice (global) nodes to nodes in VHDL-AMS depending on the simulator

- Problem:
  - Mapping between Spice and VHDL-AMS nodes
Conclusion and Further Directions

- No standard activities to „create“ VHDL-AMS models for Spice elements – if necessary extend SPICE2VHD
- Check whether
  - Standardization of a VHDL-AMS interface to Spice subcircuits and primitives is useful
  - Users are interested in it
  - EDA vendors are willing to support it
  - Other languages (Spectre, Verilog-A) should be handled in the same way
- If yes
  - Collect requirements
  - Go for same user interface in different tools
  - Avoid restrictions to vendors‘ implementations