SV-EC Status
18 September 2003

David Smith – Chairman
Neil Korpusik – Co-Chairman
Agenda

• Mission
• Members
• Status
• Milestones
• Challenges
• SystemVerilog LRM - Status
Mission

- Maintain and extend the SystemVerilog language for testbench support
### Members

#### Voting Company Members
<table>
<thead>
<tr>
<th>Name</th>
<th>Company</th>
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<tbody>
<tr>
<td>Arturo Salz</td>
<td>Synopsys</td>
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<tr>
<td>Brad Pierce</td>
<td>Synopsys</td>
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<tr>
<td>Cliff Cummings</td>
<td>Sunburst Design</td>
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<td>Dave Rich</td>
<td>Synopsys</td>
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<tr>
<td>David Smith</td>
<td>Synopsys</td>
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<tr>
<td>Dennis Brophy</td>
<td>ModelTech</td>
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<td>Jay Lawrence</td>
<td>Cadence</td>
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<td>Jeff Freedman</td>
<td>ModelTech</td>
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<tr>
<td>Michael Burns</td>
<td>Motorola</td>
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<tr>
<td>Mehdi Mohtashemi</td>
<td>Synopsys</td>
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<tr>
<td>Neil Korpusik</td>
<td>Sun</td>
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<tr>
<td>Ray Ryan</td>
<td>ModelTech</td>
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#### Non-Voting Company Members (due to attendance)
<table>
<thead>
<tr>
<th>Name</th>
<th>Company</th>
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<tbody>
<tr>
<td>Stefen Boyd</td>
<td>Boyd Tech.</td>
</tr>
<tr>
<td>Stu Sutherland</td>
<td>Sutherland HDL</td>
</tr>
<tr>
<td>Kevin Cameron</td>
<td>CPU Tech</td>
</tr>
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#### Participating Individual Members
<table>
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<tr>
<th>Name</th>
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<tr>
<td>Don Mills (LCDM)</td>
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<tr>
<td>James Young (HP)</td>
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4  18 September 2003  www.accellera.org
Status - Errata

- Errata items logged: 21
  - Closed: 8
    - C handle garbage collection
    - endianess clarification
    - clarification of using inside operator outside of constraints
    - minor typos and clarifications
  - Items in progress: 13
    - handling of automatic variables in fork..join_none/any
    - clarification of built-in class redefinition and built-in namespace
    - types and clarifications
Status - Extensions

- Extensions logged: 15
  - Moved:
    - EXT-13 to SV-BC general namespace support
  - Closed with no action:
    - EXT-5 Optional order of sign, etc...
  - Closed with no submission:
    - EXT-1 Additional string routines
    - EXT-4 Additional tasks for new types
  - Approved:
    - EXT-2 Fine Process Control (2 pages)
  - Accepted:
    - EXT-8 RandCase support (close to approval) (1 page)
    - EXT-9 Stream Generation (7 pages)
    - EXT-14 Constraint completion (11 pages)
    - EXT-15 General foreach construct (1 page)
  - Submitted:
    - EXT-3 Virtual interfaces/ports (5 pages)
    - EXT-6 Size of types (1 page)
    - EXT-7 Reacting to assertions (3 pages)
    - EXT-10 Functional Coverage Specification (10 pages)
    - EXT-11 Dynamic Queue Support (6 pages)
    - EXT-12 Bit stream support (pack/unpack) (6 pages)
  - Total additional pages: 53 (max – actually somewhat smaller due to rounding up)
Milestones

- 7 July 2003 – Committees start operating
- 4 August 2003 – Close of submission commitments
- 15 September 2003 – Close of submissions
- 1 December 2003 – Complete technology errata, freeze technology of submissions, close implementation feedback
- 24 December 2003 – End of LRM development, start of LRM review
- 24 January 2004 – Send to board
- 24 February 2004 – Release 3.1a LRM
Challenges

• 51 pages to review, refine, and approve in 11 weeks (5 pages a week)
• Keeping coordinated with other committees
  – EXT-6 has overlap
  – LRM-16 (general inside operator)
  – Others?
Status – LRM Changes

- http://www.eda.org/sv/LRMChanges.html
- Changes logged: 24
  - (1 shared between SV-BC/SV-EC)
  - SV-AC: 1 proposed
  - SV-BC: 8 accepted, 4 proposed
  - SV-CC: 2 accepted, 1 proposed
  - SV-EC: 8 accepted, 1 proposed
  - Changes include minor corrections, clarifications, plus new extensions