SystemVerilog Basic Committee

Johny Srouji (Chair)
Karen Pieper (Co-Chair)
## SV-BC Participants

### 17 Active Participants
- Tom Kiley - Mentor
- Matt Maidment - Intel
- Brad Pierce - Synopsys
- Karen Pieper - Synopsys
- Johny Srouji - Intel
- Dan Jacobi - Intel
- Dave Rich - Synopsys
- Francoise Martinolle - Cadence
- Jay Lawrence - Cadence
- Dennis Brophy - Mentor
- Vassilios Gerousis - Infineon
- Cliff Cummings - Sunburst Design
- Mark Hartoog - Synopsys
- Don Mills - LCDM Engineering
- Doug Warmke - Mentor
- Rishiyur Nikhil - Bluespec
- Stu Sutherland - Sutherland HDL

### 90 Members of Email Reflector
- Sunburst Design
- 0-in
- Infineon
- Cisco
- Verplex
- Synplicity
- Synopsys
- Parthosceva
- NSC
- Telllabs
- Xilinx
- Doulos
- Cadence
- Interra Systems
- Applister
- Bluespec
- Axis
- Boyd Technology
- LSI
- Handasarabia
- Verisity
- Expert EDA
- Motorola
- Mentor
- Willamette HDL
- LCDM
- Intel

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2 August 21, 2003 Vassilios Gerousis www.accellera.org
SV-BC Status

• Mission
  • Address remaining issues from System Verilog 3.0
  • Address issues exposed in SystemVerilog 3.1 standard through implementation
  • Handle all design modeling issues, such as refinements of the language as well as design enhancements, to solidify System Verilog as RTL design language

• Goal
  • Be complete with 3.1A release by DVCON 2004
SV-BC: Accomplishments

• Approved operating guidelines

• Received donations
  > SV-BC-37 - Interface port expressions "modport expressions.pdf"
  > SV-BC-48 - Flexibility in Function description and use
  > SV-BC-49 - Operator overloading
  > SV-BC-52 - Packing/unpacking cast (Donated to SV-EC)
  > SV-BC-53 - Expand array querying functions
  > SV-BC-54 - Changing ref ports for variables in an interface
  > SV-BC-71 - Tagged Unions

• Issue status
  > 71 issues have been filed
  > 40 (56%) have been addressed
  > 8 (11%) have proposals
  > 27 (38%) are currently open, deferred
SV-BC: Milestones

• 7 July 2003 – Committee starts operating
• 4 August 2003 – Close of submission commitments
• 15 September 2003 – Close of submissions
• 1 December 2003 – Complete technology errata, freeze technology of submissions, close implementation feedback
• 24 December 2003 – End of LRM development, start of LRM review
• 24 January 2004 – Send to board
• 24 February 2004 – Release 3.1a LRM
Separate Compilation

• Voting on a proposal to introduce “packages” to the language
  • Support separate compilation by providing non-$root mechanism for sharing types

• Will further discuss proposals:
  • Separate roots
  • Extern declarations

• Completed proposals will be sent to the SV-BC for acceptance into the standard