SV-AC Update
18 September 2003

Faisal Haque – Chairman
Arif Samad – Co-Chairman
Agenda

• Mission
• Members
• Status
• Milestones
Mission

• Incorporate feedback from EDA vendor implementations of 3.1 and customer usage
• Complete enhancements from v3.1 development required to make SystemVerilog a solid foundation for HDVL
## Members

<table>
<thead>
<tr>
<th>Voting Company Members</th>
<th>Non-Voting Company Members (due to attendance)</th>
<th>Participating Individual Members</th>
</tr>
</thead>
<tbody>
<tr>
<td>Faisal Haque (Cisco)</td>
<td>Arif Samad (Synopsys – replacing Steve)</td>
<td>Connie O’Dell (consultant)</td>
</tr>
<tr>
<td>Steve Meier (Synopsys - outgoing)</td>
<td>Richard Ho (0-In)</td>
<td></td>
</tr>
<tr>
<td>Roy Armoni (Intel)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Surrendra Dudani (Synopsys)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cindy Eisner (IBM)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>John Havlicek (Motorola)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Adam Krolnik (LSI)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Joseph Lu (Sun)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eric Marschner (Cadence)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Andrew Seabright (0-In)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bassam Tabbara (Novas)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tej Singh (Mentor)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hillel Miller (Motorola)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Status - Errata

- Errata items logged: 7
  - Closed: 6
    - Associativity – change to right
    - Allow clocked sequences (including multi-clock) to be parenthesized
    - Parenthesis around expression with local variable assignments
    - Formal semantics needs to define meaning of multiple local variables attached to a single boolean
    - Need to define neutral trace semantics, in alignment with PSL
  - Items in progress: 1
    - Unary ## should have the higher precedence than binary ##
Status - Extensions

• Extensions logged: 26
  – Moved:
    • EXT-18 General clocked event object triggered on completion of assertion (SV-EC)
    • EXT-19 Extend expect to support wait on in-lined sequence event… (SV-EC)
    • EXT-20 Feature to embed assertions within a user defined type… (SV-BC)
  – Closed:
    • EXT-17, 21
  – For consideration beyond 3.1a
    • EXT 22 – template feature (should be passed to BC)
    • EXT 23 – extend time windows to allow negative delays
    • EXT 24 - assertions on variables, classes, dynamic objects
    • EXT 25 - allow additional temporal operators…
    • EXT 26 – More fomal features
Status – Extensions (continued)

- Submitted:
  - EXT-1 – Assume directive for concurrent assertion... (Surrendra)
  - EXT-2 - Assume directive that must hold for all times (Joseph)
  - EXT-3 - Alignment/synchronization with testbench constraints language (Surrendra)
  - EXT-4 - Local variable reference outside of containing assertion (John)
  - EXT-5 - Non-blocking clocked assignment variables... (Surrendra)
  - EXT-6 - Message reporting using assertion values,... (Surrendra)
  - EXT-7 - Support parameters for assertions, extend to allow sequence... (Joseph)
  - EXT-9 - Allow passing of infinite range as argument... (Surrendra)
  - EXT-11 - Dynamic and recursive calls to a property... (John)
  - EXT-12 - Boolean connectives, nesting... (John)
  - EXT-13 - Assertions inside of functions (Adam)
  - EXT-14 – Enhance gated clock support (Surrendra)
  - EXT-15 - Report interface assertion messages in child scope... (Adam)
  - EXT-16 – Extend modport to enable assertions in modport statement (Adam)
Milestones

- 7 July 2003 – Committees started operating
- 12 August 2003 – Close of submission commitments
- 15 September 2003 – Close of submissions
- 1 December 2003 – Complete technology errata, freeze technology of submissions, close implementation feedback
- 24 December 2003 – End of LRM development, start of LRM review
- 24 January 2004 – Send to board
- 24 February 2004 – Release 3.1a LRM