SystemVerilog

Face to Face Meeting
14 November 2003
Agenda for 3.1A

• 9:00 - 9:15 - Introduction.
• 9:15 - 10:15 SV Committee Status
  15 minutes - SystemVerilog Design Committee - Johny/Karen.
  15 minutes - SystemVerilog Assertions - Faisal / Arif
  15 minutes - SystemVerilog C/API - Swapnajit / Ghassan
  15 minutes - SystemVerilog Testbench - David / Neil.
• 10:15- 10:30 Break.
• 10:30 ---- Special Topics
  Separate Compilation and Packages (David).
  SV-CC Donation Update (Swapnajit)
  Assume and Sequences in constraints (Surrendra)
  Functional Coverage (Arturo)
  BNF Status (Brad)