

The if else definition at annex F is not compatible with verilig if else

Aligned with p1800-2008-draft 4

**Motivation: if (b) P1 else P2" is defined in annex F as a shortcut to "(b |-> P1) and (!b |-> P2)". The problem with this definition is that b = X, nither P1 nor P2 are required to hold. This is inconsistent with SV procedural "if else" where the else block should be executed.**

At F.2.3.5

Replace

- ( if ( b ) P1 else P2 ) ≡ ( ( b |-> P1 ) and ( !b |-> P2 ) )

With

- ( if ( b ) P1 else P2 ) ≡ ( ( b |-> P1 ) and (~~!b~~'!bit'(b != 'b0) |-> P2 ) )