

Enhancement List for System Verilog Assertions

List of unprioritized enhancements for v3.1

Assertion Enhancements for SV-AC in SV v3.1a

Item Number	Item Name	Proposer	Type	Enhancement Description	Sub-Committee	Comittment
1	Addl_prop_directive	Steve Meier	Enhance	assume directive for concurrent assertion to be used as environment, random test generation constraint	SV-AC	Surrendra
2	immed_assume	SV-AC	Enhance	assume directive that must hold for all times (assumed immediate)	SV-AC	?
3	assume_sync	SV-AC	Enhance	alignment/ synchronization with testbench constraints language, clarify on usage/application differences	SV-AC	Surrendra
4	local_var_ext	John, Bassam	Enhance	local variable reference outside of containing assertion	SV-AC	John
5	clock_var_assign	Surrendra	Enhance	non-blocking clocked assignment variables to be assigned within assertion block	SV-AC	Surrendra
6	clock_var_access	Adam Krolnick	Enhance	Message reporting using assertion values, debug sampled variable assignments	SV-AC	Surrendra
7	param_asserts	Joseph Lu	Enhance	Support parameters for assertions, extend to allow sequence as parameter	SV-AC	?
8	seq_passing_mod	Adam Krolnick	Enhance	Extend module to support passing sequences and properties, extend port list	SV-AC	Surrendra, coord
9	inf_pass_arg	Surrendra	Enhance	Allow passing of infinite range as argument to properties and sequences, consider possibility of alternate syntax for infinite	SV-AC	Surrendra
10	enhance_implic	Surrendra, John	Enhance	Extend implication to support nesting of implication, extend implication to support nesting of implication with multiple clocks.	SV-AC	Surrendra
11	recursive_property	Hillel	Enhance	Extend properties to allow dynamic and recursive calls to a property. Support creation of recursion to dynamically create list of properties based on values.	SV-AC	John
12	bool_prop_conn	John	Enhance	support boolean connectives like conjunction (AND) on properties (possibly together with nesting)	SV-AC	John
13	temp_operators	SV-AC	Enhance	allow additional temporal operators for increased expressiveness (omega regular language)	SV-AC	?
14	formal_features	Roy Armoni	Enhance	more formal features (TBD)	SV-AC	?
14	assert_in_func	Adam Krolnick	Enhance	enable assertions to be used within functions in procedural scope. Ability to keep assertions with design code inside of funtions.	SV-AC	?
15	gated_clk_support	Adam Krolnick	Enhance	feature to support gated clock within clocking expression.	SV-AC	Surrendra
Assertion Related Enhancements Target by other Sub-Committee						
18	event_temporal	Arturo	Enhance	general clocked event object triggered on completion of assertion, handled similar to other verilog events	SV-EC	
19	expect_temporal	Arturo	Enhance	extend expect (blocking wait) to support wait on in-lined sequence event or named clocked event completion	SV-EC	
20	embed_struct	Steve Meier	Enhance	feature to embed assertions within a user defined type (typedef), assertion will be checked in every instantiation of struct	SV-BC	

Enhancements for consideration beyond v3.1a					Sub-Committee	N/A
22	template	SV-AC	Enhance	template feature (should be passed to BC)	SV-BC	N/A
23	neg_delay	Prakash/DWG	Enhance	extend time windows to allow negative delays	SV-AC	N/A