

Assertion Committee Working Group

Status March 20, 2003

Issue	Operator Function	SV 3.1 – 0.81 (Current DWG proposal)	New proposed	ACWG resolution
1	Cycle delay	; or ;[range]	##expr or ##[range]	##const ##[const] ##[const:const] ##[const:\$]
2	Cycle delay as separator		## is the separator between sequence_elements	Resolved
3	Character for separator		, between assignments and Boolean_expressions	Resolved
4	Sequential and	&&	and – use words to be consistent with other sequence operators	and
5	Sequential or		Or	or
6	Sequential intersect	intersect	No Change	No Change
7	Sequential implication	=>	No Change	No Change
8	Iterative repetition	seq * [num_or_range]	Match PSL	seq [*const] seq [* const:const] seq [* const:\$]
9	Infinite	inf	Don't like new short keywords. Better to have some character than nothing. \$ represents 'end' in many other places	const:\$
10	Occurrence repetition	bool_expr *= [num_or_range]	Same as 8	seq [*=const] seq [*= const:const] seq [*= const:\$]
11	Suffix implication	=>	No Change	No Change
12	Rising value between clocks	\$rose	\$rose becomes a reserved keyword, like \$hold, cannot be overridden by PLI	No Change
13	Falling value between clocks	\$fell	Same as 12	No Change
14	Change value between clocks	\$stable	Same as 12	No Change
15	Endpoint of sequence (same clock)	ended seq_name	seq_name . Ended Since ended is only used with an identifier, it can be a method. Method may be used with expression syntax in a sequence	seq_name . ended
16	Endpoint of sequence (different clock)		seq_name .matched Same as 13	seq_name . matched
17	First sequence	first_match(seq_expr)	Same as 12	\$first_match

	match			
18	Next Boolean event	next_event(bool_expr)	Same as 12	\$first_occur
19	Boolean holds throughout a sequence	bool_expr throughout seq_expr	One proposal has been made, but not reviewed	No change
20	Sequence occurrence within a sequence	Seq_expr within seq_expr	No Change	No Change
21	Sequence Declaration	sequence s =	sequence identifier() endsequence	Resolved
22	Property Declaration	property p =	property identifier(); endproperty	Resolved
23	Immediate assertion	check	assert. Can now use same keyword. No ambiguity with concurrent assert	assert
24	Concurrent assertion	assert cover		Resolved
25	Template Generation		One proposal has been made, but not reviewed. See below	Resolved
26	System Functions	\$countones, \$onehot, etc	These are general use system functions	Move to section 22, System tasks and functions
27	Asynchronous reset	accept(expr)	disable iff expr Clearer to Verilog users	disable iff expr