

## **Benchmark Software Documentation Table of Contents**

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## **1.0 Introduction**

This document contains a directory and description of the files for the software developed by Lockheed Sanders during RASSP Benchmark 1. Both the Ada application code and the VHDL virtual prototype code are included. It also contains information about the tools used in development and necessary to run the code.

There is an accompanying TAR file, containing `ada_deliverable.tar.Z` and `BM1_Model.tar.Z`, which incorporates the deliverable software. The TAR file also contains the directory and descriptive material found in this document.

The combination of this document and the TAR files fulfill the requirements for Data Item E001, Computer Software Product End Items, Benchmark Software Documentation.

## **2.0 Directory, Description, and Instructions for Benchmark 1 Ada Application Code**

## 2.1 Ada Software Description

The software developed on Benchmark 1 is described below. This software is currently under development, and has not been fully integrated, debugged, or tested.

The software has been organized into Ada packages, with two files per package: one file for the package specification (\*.ads) and one file for the package body (\*.adb). The only exception to this are the main programs, which include only a subprogram. They do not have a specification file. The file index.txt lists the Ada files and gives a short description of what they contain.

The software has been compiled using the Alsys AdaWorld Cross Compiler for Motorola 68K Targets, version 5.5.2, running under SunOS and Motif. The software was bound using the same tool, and it was linked using the Microtec 68K linker, version 7.0.

The software was executed using the Microtec XRAY Debugger, also called an Instruction Set Simulator, version 3.2B.

Alsys provides several board support packages (BSP). One of these BSPs is linked into the executable depending on the target. Two BSPs have been included, one for the Microtec XRAY Debugger (userx20.asm) and one for the Motorola VME 167 board (user167.asm). The linker command files are also provided in pgmxray.cmd and pgm167.cmd. These files are used by the Microtec linker to build the executables.

## 2.2 Index of Benchmark 1 Ada Files

**Table 1: Directory of Benchmark 1 Ada Files**

Filename	Description
boot.ads	This package contains the boot software.
boot.adb	This package contains the boot software.
bus_interface.ads	This package contains the low level reads and writes to hardware registers.
bus_interface.adb	This package contains the low level reads and writes to hardware registers.
command.ads	This package contains the command software.
command.adb	This package contains the command software.
convolution_kernel_p1.ads	This package contains the part 1 of 5 of the ROM convolution kernel (kernels 1 -6).
convolution_kernel_p2.ads	This package contains the part 2 of 5 of the ROM convolution kernel (kernels 7 -12).
convolution_kernel_p3.ads	This package contains the part 3 of 5 of the ROM convolution kernel (kernels 13 - 18).
convolution_kernel_p4.ads	This package contains the part 4 of 5 of the ROM convolution kernel (kernels 19 - 24).
convolution_kernel_p5.ads	This package contains the part 5 of 5 of the ROM convolution kernel (kernels 25 -31).
convolution_kernel_p1.adb	This is a stub body
convolution_kernel_p2.adb	This is a stub body
convolution_kernel_p3.adb	This is a stub body
convolution_kernel_p4.adb	This is a stub body
convolution_kernel_p5.adb	This is a stub body
default_tables.ads	This package contains only definitions.

**Table 1: Directory of Benchmark 1 Ada Files**

Filename	Description
default_tables.adb	This is a stub body for this package which contains only definitions.
defined_types.ads	This package contains data structure information shared by the various packages.
defined_types.adb	This is a stub body for this package which contains only definitions.
dsp_azimuth_vector.ads	This package contains the input and output vectors used for the azimuth DSP
dsp_azimuth_vector.adb	This is a stub body.
dsp_driver_functions.ads	This package contains control software for controlling and monitoring the DSP Interface. It communicates with the range processor, corner turn memory (CTM), azimuth processor, and Raceway interface
dsp_driver_functions.adb	This package contains control software for controlling and monitoring the DSP Interface. It communicates with the range processor, corner turn memory (CTM), azimuth processor, and Raceway interface
dsp_input_test_vector.ads	This package contains the input vector used for all DSP self-tests (range, azimuth, and slant).
dsp_input_test_vector.adb	This is a stub body for input vector self-test.
dsp_range_vector.ads	This package contains the input and output vectors used for the DSP range self-test.
dsp_range_vector.adb	This is a stub body.
dsp_self_test.ads	This package contains the self test software for the blocks on the DSP interface: range processor, corner turn memory (CTM), azimuth processor, and Raceway interface.

**Table 1: Directory of Benchmark 1 Ada Files**

Filename	Description
dsp_self_test.adb	This package contains the self test software for the blocks on the DSP interface: range processor, corner turn memory (CTM), azimuth processor, and Raceway interface.
dsp_slant_test_vector.ads	This package contains the output vectors for the slant self-test.
dsp_slant_test_vector.adb	This is a stub body.
equalization_weights_p1.ads	This package contains the part 1 of 2 of the ROM equalization weights (HH, HV polarizations).
equalization_weights_p2.ads	This package contains the part 2 of 2 of the ROM equalization weights (VH, VV polarizations).
equalization_weights_p1.adb	This is a stub body.
equalization_weights_p2.adb	This is a stub body.
foi_driver_functions.ads	This package contains control software for controlling and monitoring the Fiber Optic Interface (FOI). It communicates with the FOI and the FOI Raceway interface.
foi_driver_functions.adb	This package contains control software for controlling and monitoring the Fiber Optic Interface (FOI). It communicates with the FOI and the FOI Raceway interface.
foi_self_test.ads	This package contains the self test software for the FOI interface.
foi_self_test.adb	This package contains the self test software for the FOI interface.

**Table 1: Directory of Benchmark 1 Ada Files**

Filename	Description
main.adb main1.adb main_az.adb main_demo.adb main_demo1.adb main_foi.adb main_image.adb main_range.adb main_rw.adb main_small.adb	Main programs used to test and run various portions of the software
message.ads	This package contains the software which handles the messaging.
message.adb	This package contains the software which handles the messaging.
rs232.ads rs232_min.ads rs232.adb rs232_ctm.adb	These files contain the software which handles the RS232 interface.
slant_range.ads	This package contains the slant range task software.
slant_range.adb	This package contains the slant range task software.
tables.ads	This package contains the current data tables.
tables.adb	This contains the software which initializes the dynamic tables with the default values stored in ROM.
taylor_weights_p1.ads	This package contains the part 1 of 2 of the ROM Taylor weights (HH, HV polarizations).
taylor_weights_p2.ads	This package contains the part 2 of 2 of the ROM Taylor weights (VH, VV polarizations).

**Table 1: Directory of Benchmark 1 Ada Files**

Filename	Description
taylor_weights_p1.adb	This is a stub body.
taylor_weights_p2.adb	This is a stub body.
uart.ads	This package contains driver software for the UART.
uart.adb	This package contains driver software for the UART.

### **2.3 Instructions for Extracting the Benchmark 1 Ada Code**

This tape includes a snapshot of the deliverable Ada software that has been developed on the RASSP Benchmark. All of the files have been placed in one tar file and compressed. To extract the files:

```
uncompress ada_deliverable.tar.Z  
tar xvf ada_deliverable.tar
```

### **3.0 Directory, Description, and Instructions for Benchmark 1 VHDL Code**

### 3.1 Directory Structure of the Benchmark 1 VHDL Model

The following lists the directory structure for Benchmark 1.

**Table 2: Directory Structure for Benchmark 1 VHDL.**

Directory	Description
source	All source code
source/bm1_math	MIT Lincoln Labs Benchmark 1 Math source code
source/vsd2dat	MIT Lincoln Labs Benchmark 1 Non-math source code
source/bm1_source	Sanders Benchmark 1 SAR source code
source/bm1_source/corner_turn	Sanders Benchmark 1 Corner Turn source code
source/bm1_source/fo_interface	Sanders Benchmark 1 Fiber Optic source code
source/bm1_source/packages	Sanders Benchmark 1 Packages source code
source/bm1_source/race_controller	Sanders Benchmark 1 Race Controller source
source/bm1_source/sanders_sar	Sanders Benchmark 1 top level source code
source/bm1_source/sar_lite	Sanders Benchmark 1 SAR Lite source code
source/bm1_source/testbench	Sanders Benchmark 1 Testbench source code
source/bm1_source/vme	Sanders Benchmark 1 VME source code
lib	Default compile area
lib/bm1.lib	MIT Lincoln Labs Benchmark 1 Math library area
lib/bm1_math.lib	MIT Lincoln Labs Benchmark 1 Non-math library area
lib/vsd2dat.lib	Sanders Benchmark 1 SAR library area

### 3.2 File Description of the Benchmark 1 VHDL Source Code

The Files are found in source/bm1\_source. The following is a list of the VHDL files for Sanders Benchmark 1 SAR source code.

**Table 3: Benchmark 1 VHDL Source Code**

Filename	Description
MakeSandersSar	Benchmark 1 Makefile for Compilation of Sanders_Sar Model
azimdsp-a-behave1.vhd	Azimuth DSP Behavioral Architecture
azimdsp-e.vhd	Azimuth DSP Entity
azimdsp_tb-e-a.vhd	Azimuth DSP test bench - processing mode
azimdsp_tb2-e-a.vhd	Azimuth DSP test bench - test mode
bm1package-b.vhd	Benchmark 1 Package Body
bm1package-p.vh	Benchmark 1 Package Declaration
ctm-a-bfm.vhd	This file contains the behavioral architecture for the Corner Turn Memory Model
ctm-e.vhd	Corner Turn Memory (CTM) Entity
ctm_rcv_test_tb.vhd	This test bench exercises the receive test mode circuitry embedded within the Corner Turn Memory model. During the receive test mode, the Corner Turn extracts data out of the Range DSP's Sync fifo and loads it into an output register.
ctm_tb.vhd	This test bench exercises the functions of the Corner Turn Memory under normal operation. Data is passed to the Corner Turn Memory from the Range DSP. The data is temporarily stored by the Corner Turn's DRAM and then sent to the Azimuth DSP for processing. This test bench exercises the handshaking between the DSPs and the Corner Turn Memory, as well as validating the local bus interface which is used to configure the circuitry.

**Table 3: Benchmark 1 VHDL Source Code**

Filename	Description
ctm_xmt_test_tb.vhd	This test bench exercises the transmit test mode circuitry embedded within the Corner Turn Memory model. During the transmit test mode, the Corner Turn receives data through its input test registers and loads it directly into its Sync Fifo.
fiber_port-a-bfm.vhd	Fiber Port Behavioral Architecture
fiber_port-e.vhd	Fiber Port Entity
fiber_port-tb.vhd	This test bench is designed to test the functionality of the fiber_port-e.vhd and fiber_port-a-bfm.vhd
foi_data_in.data	Data file for the fiber_port testbench
FiberIn.data	Data file for the fiber_port testbench
intmathpackage.vhd	Integer math package
pseudo_processor-a-bfm.vhd	Simulates the functions of a micro-controller
pseudo_processor-e.vhd	(Pseudo-) Processor Interface ENTITY
raceway-a-bypass.vhd	This architecture describes the race way interface as purely a passive device.
raceway-e.vhd	Race Way Entity
rangedsp-a-behave1.vhd	Range DSP Behavioral Architecture
rangedsp-e.vhd	Range DSP Entity
rangedsp_tb-e-a.vhd	Range DSP test bench - processing mode
rangedsp_tb2-e-a.vhd	Range DSP test bench - test mode
sanders_sar-a-structural.vhd	sanders_sar structural architecture
sanders_sar-c-structural.vhd	sanders_sar configuration

**Table 3: Benchmark 1 VHDL Source Code**

Filename	Description
sanders_sar-e.vhd	sanders_sar entity
sar-a-struct.vhd	Synthetic Aperture Radar (SAR) Processor Structural Architecture
sar-c-struct.vhd	Synthetic Aperture Radar (SAR) Processor Configuration
sar-e.vhd	Synthetic Aperture Radar (SAR) Processor Entity
sar_tb.vhd	Testbench for the SAR processor. Reads and writes files, sources data and commands, sinks data and checks latency and data magnitude.
sar_lite-a-data_flow_only.vhd	High level test version of the SAR LITE System Model
sar_lite-a-struct.vhd	SAR LITE System Model.
sar_lite-c-struct.vhd	SAR LITE System Model Configuration
sar_lite-e.vhd	Synthetic Aperture Radar (SAR) Processor Entity
tb_bfdsp.vhd	BFDSP Testbench Entity and Architecture
tb_ctm_only.vhd	BFDSP Testbench Entity and Architecture
tb_demo.vhd	18th Month Review Demo Test Bench
tb_fo_interface.vhd	Fiber Optic Interface Board Testbench
tb_pseudo_processor.vhd	Pseudo-Processor Testbench Entity, Architecture, and Configuration
tb_sar_lite.vhd	Sar Lite Testbench Entity and Architecture
tb_vme_master.vhd	VME Master Testbench
top.vhd	Ties together bm1.vhd and sar_tb.vhd.
vme_master-a-bfm.vhd	VME Master Backplane Architecture
vme_master-e.vhd	VME Master Backplane Architecture
vme_slave-a-bfm.vhd	VMEbus Slave Controller

**Table 3: Benchmark 1 VHDL Source Code**

Filename	Description
vme_slave-e.vhd	VME Slave to Local Bus Master

### 3.3 Instructions for Creating the Benchmark 1 Model

The file `bm1.tar.Z` contains all the source files needed to build the Benchmark 1 model. To compile the Benchmark 1 model perform the following steps:

- 1) `uncompress bm1.tar.Z`
- 2) `tar -xvf bm1.tar`
- 3) `source compile_bm1.scr`

It is assumed that you have at least Vantage version 5.101 and have `gmake` available