RAPID PROTOTYPING OF APPLICATION-SPECIFIC SIGNAL PROCESSORS (RASSP)

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ABSTRACT

RASSP will dramatically reduce the obsolescence of new electronic systems at their introduction and will maintain their technological currency over an extended life cycle. The four-year program will evolve and continually improve a design environment capable of yielding four times reduction in digital electronics design cycle time along with a similar improvement in quality. Success will be demonstrated with the rapid development and easy model-year upgrade of an image signal processor for an infra-red search and track (IRST) application. Additional RASSP design environment (RDE) feedback and proof will be obtained through a series of beta site evaluations and benchmarks assessments.

INTRODUCTION

RASSP will “reinvent the process by which embedded digital signal processors are designed, manufactured, upgraded and supported” [1]. Accomplishment of this objective requires the balanced application of design methodology, design automation, and processor architecture as depicted in Figure 1. All three are necessary to achieve the four times reduction in cycle time and similar improvement in fitness-for-use and cost. The best design automation system in the world will be useful only when combined with a rapid and disciplined design methodology. Similarly, processor architectures that allow model-year upgrades are key to riding the commercial technology advancement curve. Architectures that make the incorporation of the latest state-of-the-shelf elements routine, combined with rapid and disciplined design methodology and world-class Electric Design Automation (EDA) tools, will yield the improvements demanded by RASSP. In short, design the right processors, using the right tools, well.

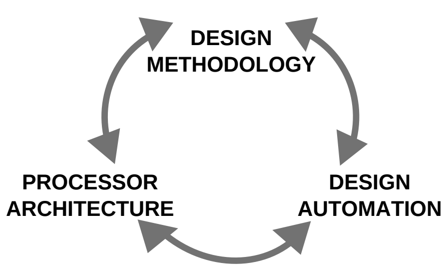

Figure 1. The balanced RASSP program. (See [1]).

PROGRAM STRUCTURE

The overall RASSP program has four major elements, some of which have more than one contractor. These elements are Primary Development, Technology Base, Benchmarker, and Educator/Facilitator. Lockheed Sanders leads one of the Primary Development efforts, with Hughes Aircraft, Motorola, Inc., and ISX as teammates. Hughes also has one of the Technology Base Development programs. Figure 2 depicts the relationships among the major program elements, all of which are managed by ARPA with the support of the three military services.

INTEGRATED PROCESS AND PRODUCT DEVELOPMENT TEAMS (IPPDT)

Figure 3 shows the Integrated Process and Product Development Team (IPPDT) program structure adopted by the Lockheed Sanders RASSP team. Each of the four teams—Systems, Design Environment, Demonstrations, and Proliferation—is led by one of the four team member companies and has members from all four companies. This leads to the concept of single responsibility/shared execution. This structure also results in a “virtual corporation” with “electronically collocated” work groups. Each team member works from his or her own office regardless of its geographic location and is connected to the rest of the team using the Internet for e-mail, video conferencing, document sharing, and collaborative work. In the paragraphs that follow, selected portions of the work product of each of these four teams will be described.

System Methodology and Process Improvement

Historically, alternative product development processes can be characterized on a continuum with very rapid on one end and highly disciplined on the other extreme. The

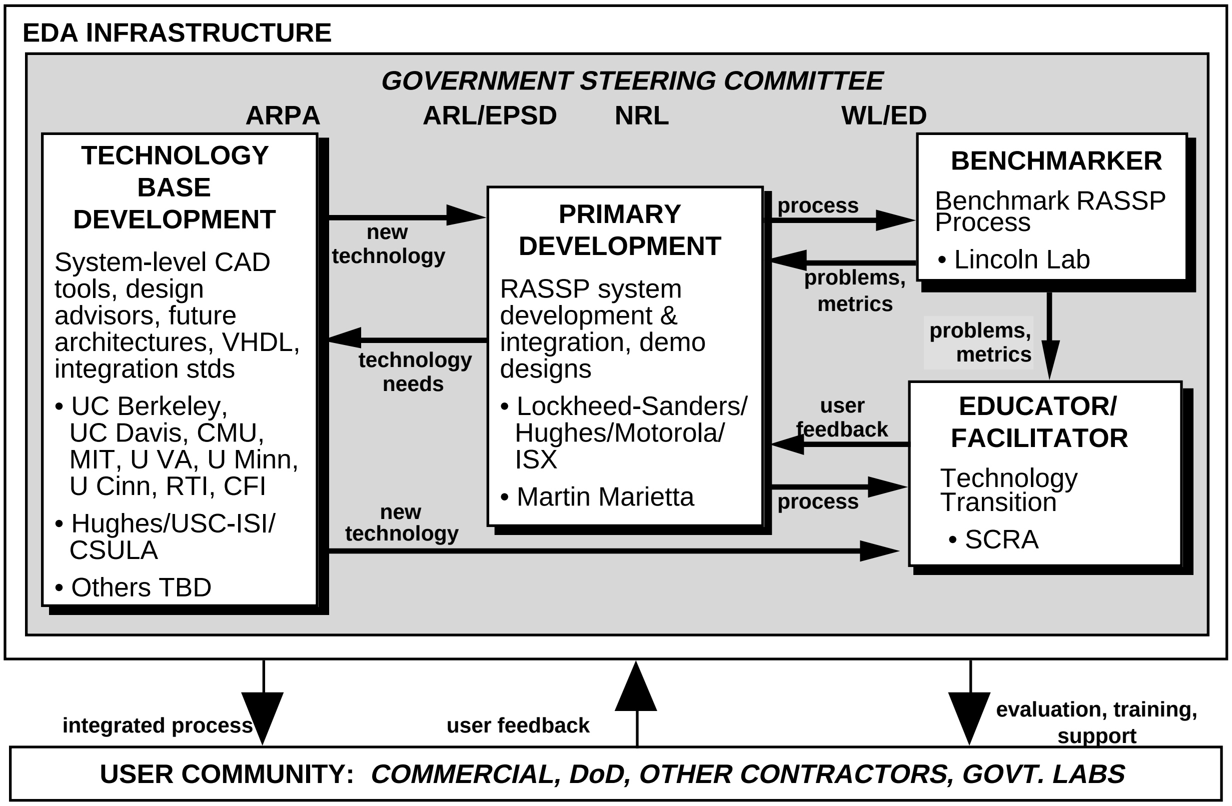

Figure 2. Major program elements and relationships (Adapted from [1])

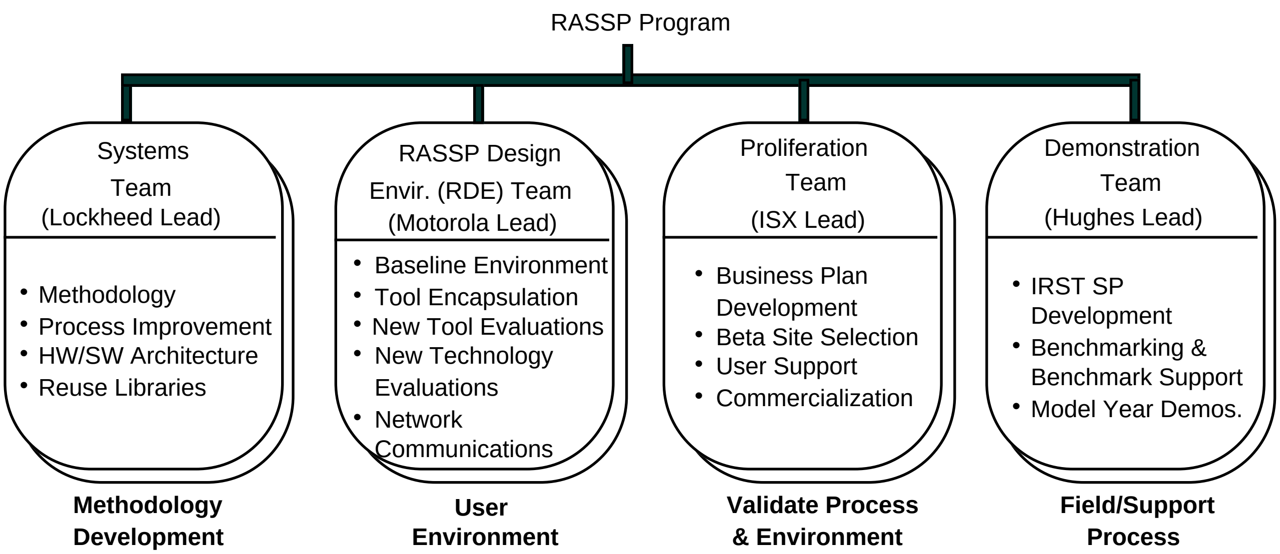

Figure 3. The Lockheed Sanders RASSP team is made up of four Integrated Product and Process Development Teams (IPPDTs) (Adapted from [2])

rapid alternative, sometimes referred to as “skunk works” or “tiger teams,” involves assembling a relatively small number of people in a common location and giving them a nearly impossible task with an exceptionally short schedule. The resulting process emphasizes speed and immediate output. Very concentrated communication occurs and each team member accepts incomplete work from other teammates to allow tasks to start early and thereby attain the shortest possible schedule. In this environment, rigorous documentation, formal review, and disciplined configuration management are replaced by intense verbal communication, on the spot review, and informal "notebook tracking." The benefits can be enormous: high performance and a one of a kind product to satisfy a critical need in a very short time. The disadvantages lie in the lack of a reusable record of what was accomplished, making the transition to quantity production difficult, time consuming, and expensive.

The opposite extreme trades speed for insurance that the product will be capable of quantity production. Each step along the way must be completed, documented, and checked for correctness prior to initiation of the next step. This highly disciplined approach leads to a very mature product that can be produced and fielded without surprises. Unfortunately, the development time involved often causes the final product to be one or more generations behind the current technology. Further, in the rapidly changing world of today, the original threat may have evolved sufficiently to make the product no longer satisfactory for the new mission.

Our approach to the RASSP engineering process involves capturing the best of these two approaches. Our Rapid and Disciplined process captures the "get started as soon as possible" characteristic of the tiger team by making the incremental release of unfinished work product simple and easy. At the same time, the disciplined tracking of requirements, design data, performance estimates, cost, schedule, product decisions, and trades is accomplished using the product data management capabilities of the RDE. The incremental release of work-in-progress includes measures of data maturity, which make it easy for subsequent users to know how far they can proceed without incurring unacceptable risk. Each person goes as far as they can with what is available, and the RASSP design environment (RDE) provides the tools for the disciplined tracking of both exit and entry criteria as the design moves from one process step to the next.

RASSP Design Environment

The Lockheed Sanders RASSP Design Environment IPPDT will develop, integrate, and demonstrate a complete environment that will make it easy for product developers to create products. The RASSP framework is a distributed software environment running on heterogeneous platforms that enables integrated product development by geographically dispersed teams. An in-depth discussion of the RDE can be found in J. Summers' paper from the first annual conference on the Rapid Prototyping of Application-Specific Signal Processors [3].

The RASSP framework provides product developers with design automation tools, process management services, and data management services. The design automation tools allow developers to accomplish their individual tasks quickly and efficiently. The process management services guide and coordinate product development teams through the development process, ensuring that parallel sets of activities occur in the correct sequences, that no activities are skipped, and that progress is clearly communicated. The data management services track and communicate the maturity of product descriptions as they progress through the process, ensuring that product developers have easy access to the data they need when they need it, that they are using the correct versions and configurations of the data, that problems are properly identified, and that changes are recorded and tracked.

RASSP Proliferation

The Proliferation IPPDT on the Lockheed Team has the task of ensuring that our RASSP process successfully transitions to other organizations and companies. This team works with the Educator/Facilitator contractor and with standards organizations such as CFI, SAE, and IEEE. Additionally, they provide an interface to the University and Industrial Technology Base contractors (see Figure 2).

The Lockheed Sanders, Hughes, Motorola, and ISX RASSP Team understands that a key element to the successful proliferation of RASSP entails an Active Electronic Marketplace^{SM} (AEM^{SM}).

Figure 4 diagrams the Active Electronic Marketplace infrastructure. The Enterprise Framework (EF) provides a common, standard user interface and enables access to all distributed project data by any legitimate user. Our approach is:

- Open – multiple hardware platforms and tools are networked into a single environment.
- Flexible – methods, processes, and tools can be modified to provide the best solution for any application.
- Adaptable – directed by the needs of an expert user community that is actively driving commercial CAD vendors for improved solutions to signal processing problems.
- Distributed and commercially available – the client-service architecture is implemented on a commercial communications net using Motif user interfaces.

Advanced, Space-Time Adaptive IRST Signal Processor Demonstration

Unambiguous proof that the RDE, associated processes, and signal processing architecture yield a four times reduction in cycle time comes from the Demonstration portion of the program, shown in Figure 5. This section will elaborate on the Lockheed Sanders RASSP Team approach to the Demonstration portion of

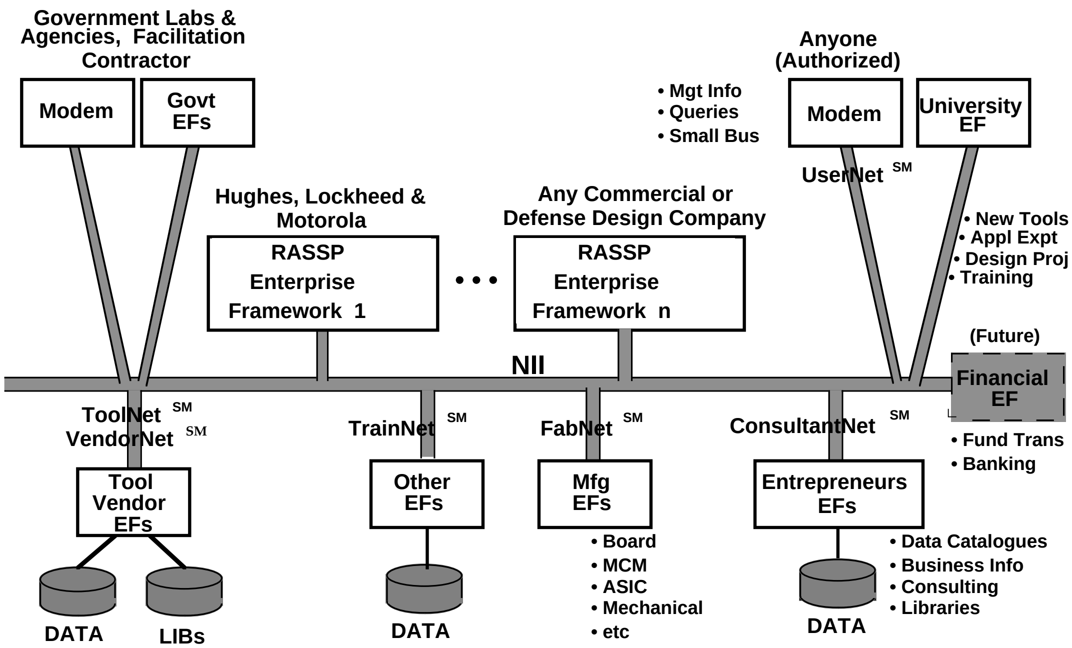

Figure 4. Active Electronic Marketplace (AEM)

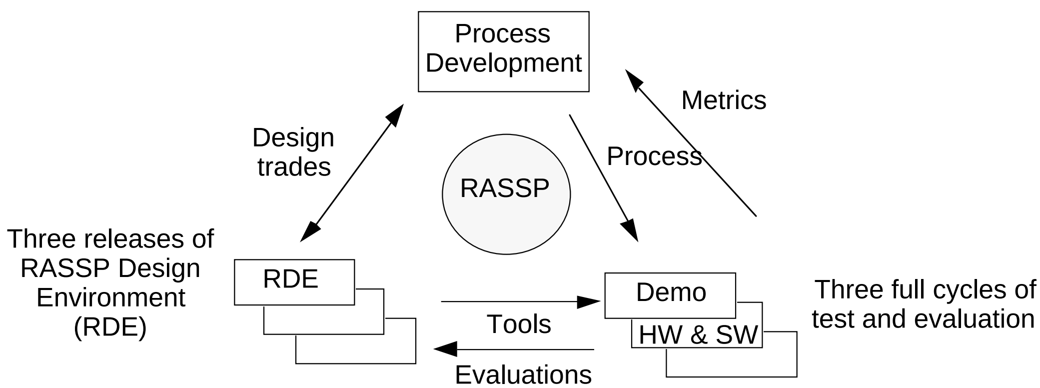

Figure 5. RASSP program elements

the program and will describe how the development of an advanced, space-time adaptive infrared search and track processor will evaluate and provide feedback for improvement of the RDE.

Demonstration Objectives

The objectives of the RASSP demonstration are to:

- Use an embedded signal processing system as a test case, spanning the development cycle from concept to specification, architecture analysis, design, manufacture and support, so that the entire RASSP process can be evaluated as it evolves during the contract.
- Design the system using the RASSP model year concept—the ability to upgrade system design rapidly and often, incorporating the latest technology and incrementally upgrading the system throughout its life cycle.
- Provide process metrics and lessons learned for methodology and process refinement. Measure the progress toward reducing product development time by a factor of four.
- Provide feedback on the usefulness of specific tools and the design environment.
- Provide clear, convincing data that RASSP methodology is practical and effective for complex design tasks.

The guiding principles for the RASSP demonstration are:

- Follow the RASSP methodology and use the RASSP toolset.
- Demonstrate completeness by showing the application in operation.

- Collect effectiveness metrics and lessons learned for improvement.
- Demonstrate processor performance growth and design cycle improvement with each model year.

RASSP Process

The Lockheed Sanders demonstration team is employing the following key elements of the RDE:

Top-down Design Refinement [4,5]. Work is released for lower level design before the current level of definition is complete. Workflow management tools will aid in this coordination.

Requirements Capture Using Domain Analysis. Domain analysis helps build reusable elements for subsequent model years and evaluates the performance of library building blocks.

Design Trades. Tradeoffs assess implementation alternatives that meet design requirements. Reuse libraries containing Ada and VHDL influence the design trades.

Standard Language. VHDL and Ada support reuse and provide the long-term stability of a standard language, which will permit parts replacement long into the future.

Simulation. Simulation satisfies two goals: 30-year supportability and perfect integration (no mistakes). As trade analyses are completed, performance level is simulated to ensure system timing. Progressive refinement defines and checks interfaces, functions, and interconnects of components. The simulation tasks build a complete hardware and software virtual prototype of the processing system.

Virtual Prototype. The virtual prototype is the climax of the first phase of the development cycle. It confirms that all design decisions are viable and that customer needs are met. It tests the hardware and software design elements together, reducing the number of errors at this interface.

Build. After complete checkout of the virtual prototype, the hardware design goes to physical design, fabrication, rapid parts procurement, and checkout. Software design changes are finalized. Hardware and software are integrated in the laboratory and then in the final system.

Model Year Upgrade. The state-of-the-shelf design replaces the state-of-the-art design. Building the system with available technology from reuse libraries, current vendor parts, portable software elements, and scalable multiprocessor architectures accelerates the design cycle. RASSP supports rapid replacement of design elements with new, faster, improved elements in subsequent design cycles. This rapid upgrade provides higher performance fielded systems and faster development schedules.

Demonstration Vehicle

The demonstration vehicle for the Lockheed Sanders Team is an airborne infrared search and track (IRST) processing system using programmable processors. It employs a heterogeneous multiple instruction multiple data (MIMD) architecture using commercial off the shelf (COTS) processor chips, operating systems, and system software tools.

The IRST processes infrared imagery at data rates up to 135 Mbytes per second. Input data are 12- to 16-bit fixed point values; however, arithmetic processing for the IRST tends to be largely floating point. Data structures are primarily multiple 2-D arrays of imagery and intermediate processed data. Array structures range from sensor size (2.2K $\times$ 1.8K pixels) to working files (200 $\times$ 100 pixels).

Throughput for the IRST will be 2 to 5 billion (achievable) operations per second.

Figure 6 shows the primary algorithms applied to IR imagery to detect and track targets in heavy clutter from a moving platform. For light clutter and fairly stationary sensors, some simplification is possible. The highlighted boxes are required in any system.

The demonstration plan calls for three model-year developments. Each model year has many of the same process steps as previous years, allowing measurement of process improvements. A factor of four improvement is expected in design cycle time during the four-year RASSP contract.

The demonstration will build increasingly complex designs within decreasing design periods. The first year, called model year 0, will build the initial libraries, software, and multiprocessor architecture. Model years 1 and 2 will demonstrate incremental upgrade and obsolete part replacement. The intent is to upgrade processing elements, algorithms, and packaging, thereby lowering power dissipation and improving throughput density as needed for application to fighter aircraft. This effort will be supported by reusable hardware and software modules. In addition, the software design will demonstrate portable, scalable software. Reference [6] provides additional detail on the hardware and software planned for the model years.

AIRMS: First External Use of RASSP Technology

The ARPA-owned Airborne Infra Red Measurement System (AIRMS) aircraft [7] will be the first platform to use RASSP-designed electronics. This Boeing 720B test aircraft houses a 24-inch aperture IR sensor. Growth racks provide more than adequate space to house the RASSP processor packaged using VME form factor.

Besides using the RASSP program designs, the AIRMS program plans to apply RASSP methodology and tools to design two electronic cards that replicate the sensor videoand transmit it to the processor. This is the first use of the of the RASSP process outside the RASSP program.

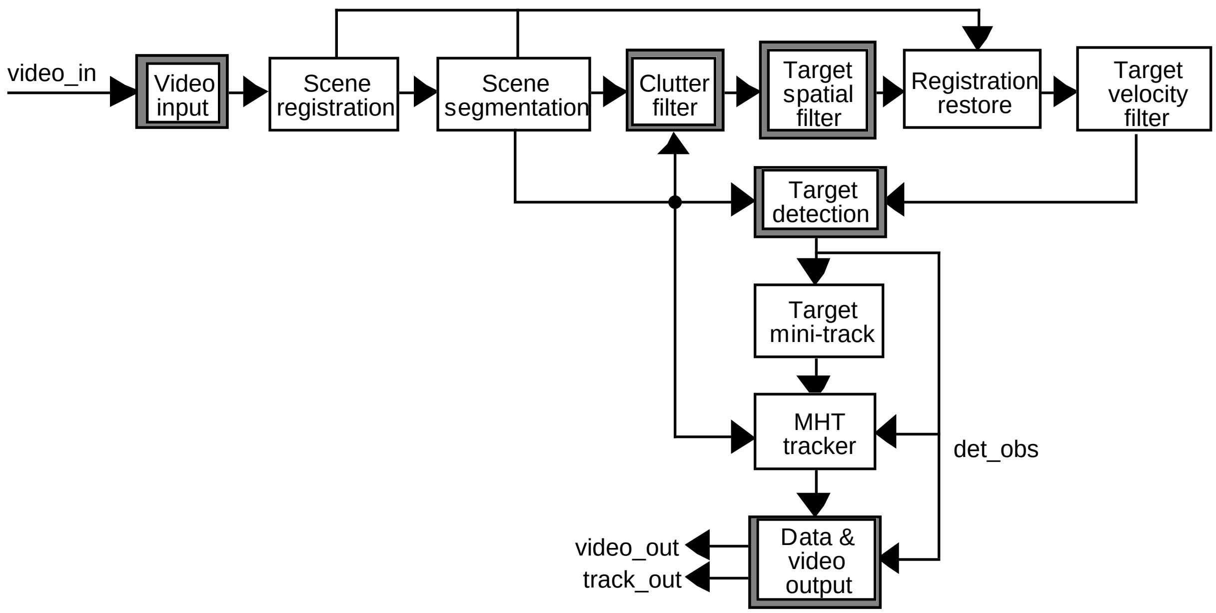

Figure 6. Primary algorithms for IR imagery analysis

The AIRMS program will fund its own copy of t aircraft, and flight tests. Initially, a subset of the processor will be built and used for closed loop tracking. Later, more processor modules are planned for additional IRST throughput.

The AIRMS application has provided specific, stressing requirements that have driven the RASSP demonstration design successfully to test the virtual prototype and rapid fabrication processes.

ACKNOWLEDGMENTS

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