

THE RAPID PROTOTYPING OF APPLICATION SPECIFIC SIGNAL PROCESSORS (RASSP) PROGRAM: OVERVIEW AND STATUS

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Introduction

The Rapid Prototyping of Application Specific Signal Processors (RASSP) program is a new four and one-half year, \$150 million ARPA/Tri-Service initiative intended to dramatically improve the *process* by which complex digital systems, particularly embedded digital signal processors, are designed, manufactured, upgraded, and supported. RASSP seeks an improvement of at least a factor of four in the time required to take a design from concept to fielded prototype or to upgrade an existing design, with similar improvements in design quality and life cycle cost. The motivation for RASSP is the need to provide affordable embedded signal processors for a wide range of DoD systems that are state-of-the-art when they are fielded, rather than when they are first defined.

This paper introduces the program from two viewpoints. The first is technical, covering the major concepts upon which the proposed RASSP approach to design is based. The second is programmatic, covering the roles of the various program participants and the status of the program as of this writing (March 1994).

Technical Themes

RASSP is not simply a program to develop electronic design automation (EDA) tools for embedded digital signal processors. The best tools in the world will not achieve good results if they are used poorly, or if they are used to design a poorly conceived product. As shown in Fig. 1, achieving the RASSP program goals will require a coordinated approach to signal processor architecture, design methodology, and EDA. Keeping the program tractable requires a strong focus on a specific problem domain. Determining whether the program goals have been met will require a comprehensive approach to evaluation of the RASSP design environment.

It is also important to realize that RASSP is not focused on the design of application specific integrated circuits (ASICs) or even of board-level products. Instead, RASSP is focused on the design of larger electronic *systems* that will typically encompass multiple boards, a variety of implementation technologies and interfaces, and a wide range of data rates.

The following sections describe the RASSP program approach to architecture, design methodology, and EDA tools for embedded signal processors.

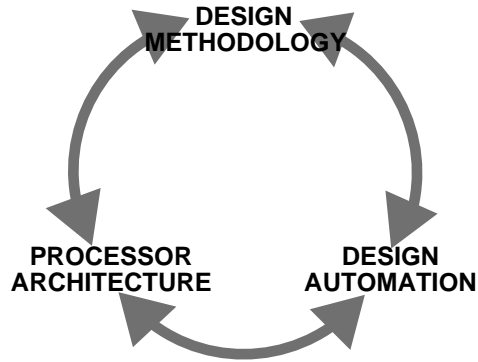


Figure 1. The RASSP program combines research in signal processor architecture, design methodology, and design automation tools.

The Model Year Concept of Design

Traditional Department of Defense (DoD) signal processor design practice emphasizes development of the best possible technology at the time of initial design. This approach, sometimes derided as the “gold-plated point design,” often implies the development of non-standard custom hardware, interfaces, and software in an attempt to maximize performance. Custom design requirements in turn lead to very long development cycles, so that prototypes are slow to get into the hands of users for operational evaluation as shown by the line marked “point design” in Fig. 2.

RASSP advocates an alternative “model year” design methodology which depends on a successive refinement approach. This method, represented by the lines marked “MY1” (“model year 1”) through “MY4” in Fig. 2, builds an initial baseline design based on a subset or relaxed set of specifications, primarily using existing hardware and software technology. The resulting prototype can be delivered to the user for test and evaluation much more quickly. The design is then upgraded, correcting any functional errors and inserting more recent technology. In the same total amount of time required to field the point design, the model year approach may evolve through several design cycles.

The model year methodology assumes the performance of available commercial technology improves rapidly, as indicated by the “commercial technology curve” in Fig. 2. So long as this remains true, a model year design approach which substitutes several short design cycles for one long cycle will end up with better performance than the point design, even if the initial baseline design must sacrifice some desired performance. Improved performance is achieved with much less reliance on expensive, difficult-to-support custom hardware and software.

The user gains from the model year approach in several ways. He or she obtains a higher-performance signal processor at a lower design cost. The processor has lower life cycle support costs because it is based on standard technology and can be upgraded as required to track supportable technology. The user also is provided prototype hardware and software early and often, by way of the evolving model year prototypes. This provides a means for uncovering flaws in the system specifications

while they are still correctable, resulting in an ultimate product better suited to the user's needs. The user becomes part of the development process in the RASSP model year design paradigm.

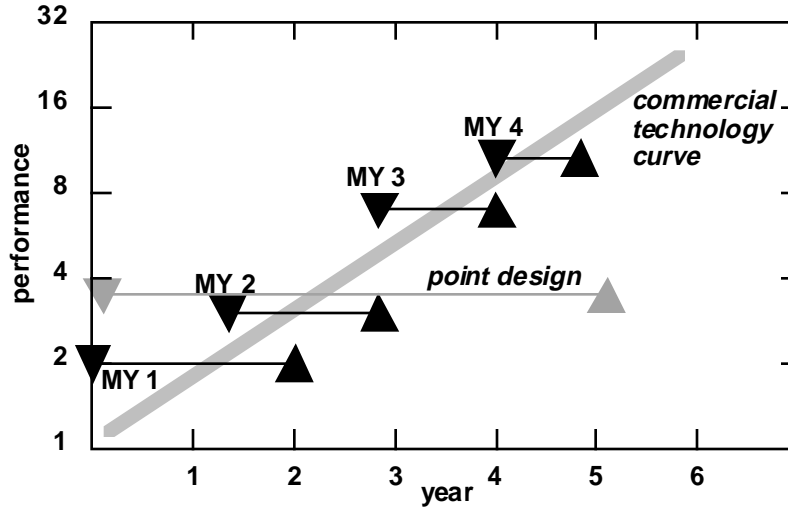


Figure 2. Comparison of point design and model year design approaches.

RASSP Architecture

The model year approach will not be efficient unless each design cycle is able to build upon the previous cycle. Each model year must not start from scratch. Consequently, the processor architecture must promote modular design and re-use of hardware and software, allowing upgrades of portions of the processor without requiring re-design of the entire system. These lessons have long been understood in the software community; RASSP seeks to apply the same concepts to embedded hardware.

Figure 3 illustrates a conceptual, high-level RASSP architecture. First is an analog front end which typically interfaces to a sensor such as a radar, sonar, or infrared device, and includes the analog-to-digital converters. The second section is the “digital front end,” which may include relatively non-programmable, high-speed hardware such as field programmable gate arrays (FPGAs) or custom application specific integrated circuits (ASICs). The third portion is a fully programmable embedded processor comprised of commercial off-the-shelf digital signal processors (DSPs), reduced instruction set computer processors, and other standard parts. These subsystems are connected with interconnect fabrics (wires, buses, crossbars, fiber optic lines, etc.) based on scalable, open hardware designs and software communication protocols. This approach of modularized hardware with standard interfaces between modules localizes the influence of a change in the design of any one portion of the system.

The key point is that RASSP is not biased to any one design approach, such as ASICs or programmable devices. Instead, it is assumed that the RASSP design system must be able to handle combinations of custom, hardware programmable, and software programmable implementation technologies, and furthermore that the technology used for a given product may evolve over multiple model years. For example, functions

originally implemented in an FPGA to meet speed requirements may be absorbed into software when a more powerful processor is instantiated in a future model year upgrade.

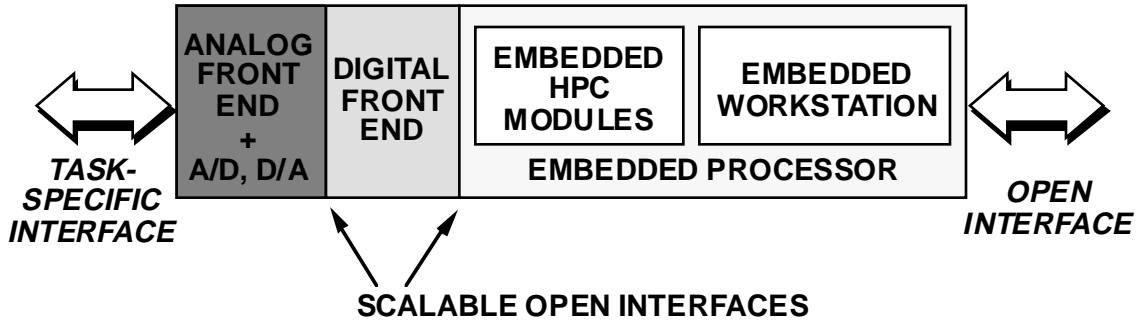


Figure 3. Conceptual RASSP architecture.

RASSP Design Flow

The biggest single challenge for the RASSP program is to develop the comprehensive, integrated, and efficient EDA system for signal processor design. It must support the designer from the earliest requirements capture to the most detailed board and ASIC design, providing full requirements traceability and virtual prototyping and an easy transition to the manufacturing process. Figure 4 illustrates one view of a RASSP design flow. Design begins with requirements capture. Next, a functional design comprising algorithms and control is developed which meets the requirements but does not specify which functions are implemented in hardware and which in software. That partitioning of the functional design occurs next. Major architectural tradeoffs are explored at this stage, such as what portions of the hardware (if any) must be hosted in ASICs, or what portion of the software (if any) must be written in assembly language. These basic decisions will have major downstream implications for performance, cost, supportability, and so forth. The design of the hardware and software is then refined and evaluated. The process of functional specification, partitioning, and preliminary hardware and software design and evaluation is iterated as required in a process called hardware/software codesign in order to obtain a solution which meets performance requirements within such constraints such as cost, form factor, power, *etc.*

At each stage of the design, virtual prototyping is used to explore design options and ensure specifications compliance and traceability. Initially the virtual prototype is entirely software, but as the design progresses, it includes hardware for an increasing number of subsystems until the final implementation is developed. Virtual prototyping requires advanced hardware and software co-simulation technology, such as the ability to mix different models of computation (for example, synchronous data flow and discrete event tokens), and the ability to have simulation tools, emulators, and hardware interact through simulation backplanes.

The RASSP design concept relies heavily on synthesis and re-use of both hardware and software modules as a means to gain efficiency in the design process. A

comprehensive database system which supports multiple views of the design data at all stages of the process is required to support this approach.

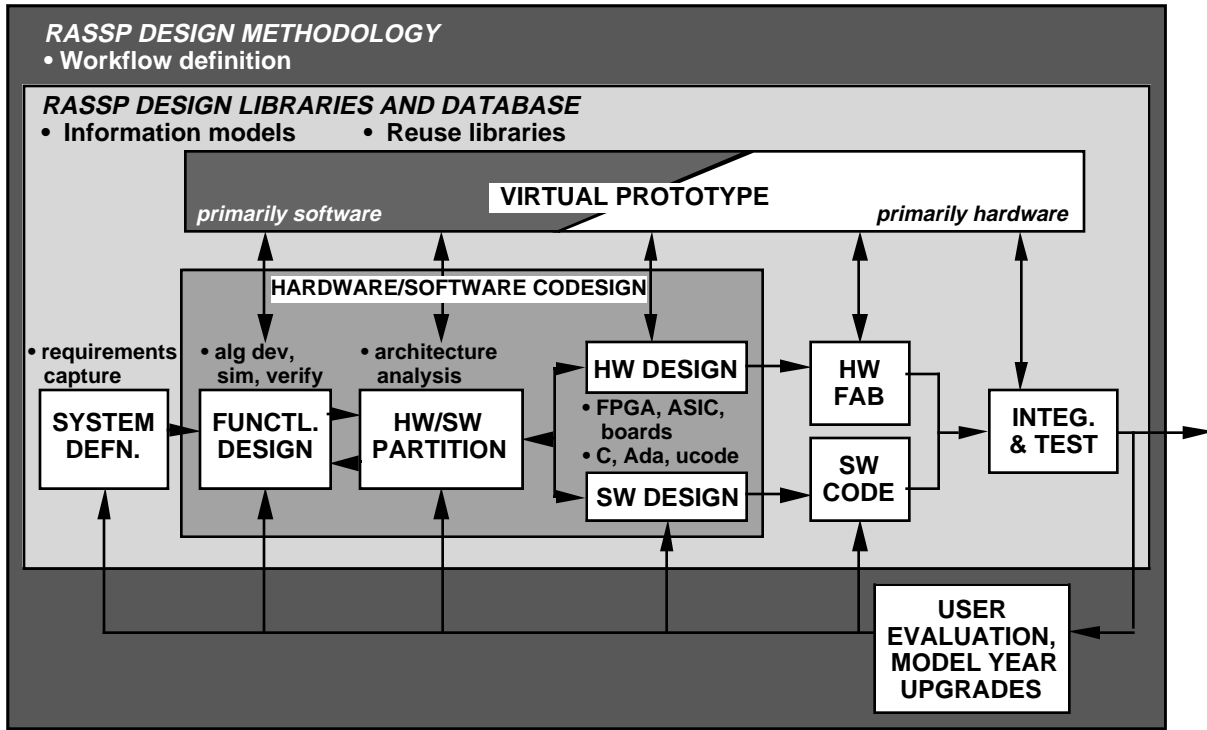


Figure 4. A view of the RASSP design flow to be implemented with electronic design automation.

RASSP is relying heavily on the VHSIC Hardware Description Language (VHDL) as a unifying design representation language and tool integration approach at the systems engineering level. The increasing acceptance of VHDL in the EDA industry, particularly for register-transfer level representations and below, make this a good language to build on. RASSP is exploring the feasibility of using VHDL-based simulatable specifications as a component of the processor requirements specification. Such a VHDL specification implicitly represents both hardware and software functionality. This specification is then expanded, refined, partitioned into explicit hardware and software modules, and ultimately used as input to synthesis tools or reuse libraries. One advantage of this approach is the ability to specify a test bench at the highest level of system definition, and then extract more detailed tests from this "master test" as the design is refined, all the while maintaining traceability to the original system-level test. Included in this work are efforts under the RASSP technology base program to explore incorporation of constraints such as form factor or power into VHDL extensions.

A complete RASSP design environment will also include many high-level systems engineering EDA tools not explicitly called out in Fig. 4. Examples include pricing models, design advisors to support early architectural decisions, tools for "ilities" analysis (e.g., reliability, maintainability), documentation and report generation, and so forth.

Currently available computer-aided design and computer-aided software engineering tools used for hardware and software design are relatively mature. Efforts at integration of tools across design levels and vendors are still in their infancy. Some tools exist for higher level requirements capture, functional specification, algorithm development, and so forth, but they are not as mature and are not well integrated with one another or with the lower level tools. Consequently, much of the actual effort under RASSP is directed towards these higher level tools.

Domain-Specific Design

Clearly, the RASSP design environment is intended to be very comprehensive. To avoid the trap of trying to develop one design environment for all electronic systems, the program concentrates on one specific problem domain to pare down the breadth of designs which must be supported. That domain is embedded digital signal processors. It is sufficiently broad to include products useful to a wide variety of DoD systems, but narrow enough to have fairly unique characteristics which can be used to advantage.

Signal processor design draws upon a base of supporting architectural, methodology, and design automation technology. Architectural approaches well-suited to real-time signal processing are usually significantly different from those used in general purpose data processing. The design methodology can be used effectively for a broader range of electronic systems. Finally, much of the EDA software and technology supports a wide range of electronic systems. Although RASSP is specific to DSPs, the base technology is applicable in large part to other problem domains as well. Consequently, much of the RASSP technology development should prove useful to other DoD and commercial electronic design domains.

Design Exercises

Goals of the RASSP program include dramatic improvements in design cycle time and affordability, and evaluation of the model year design methodology. Included are an extensive set of design efforts intended to exercise the RASSP design environment early and often on problems of real interest covering a wide range of architectures, applications, and performance levels. The results will establish a track record for the RASSP design system. The two types of design exercises are system demonstrations and benchmarks.

System demonstrations are specific processor designs, proposed and performed by the primary development contractors, and intended to be actually usable in a DoD weapon system. Demonstrations proceed through two to four model year cycles, and result in prototype hardware and software suitable for insertion into a fielded system.

Demonstrations also provides a low cost way for third parties such as DoD program offices or other federal agencies to participate in the RASSP program by funding a design of their own specification as a program add-on. The agency takes advantage of the ARPA investment in the RASSP design environment to develop an advanced signal processor while paying only the costs specific to their design.

Benchmarks are more modest and more generic but still DoD-relevant designs proposed by the benchmarking contractor in cooperation with the government steering committee and the primary development contractors. Benchmark exercises will result in products in either virtual or actual prototype form. The RASSP benchmark contractor

will verify that the products meet specification, but the real thrust of this program activity is to collect benchmark information on the design *process* used to create the product.

Six to seven semiannual benchmark designs are planned for the RASSP program. The total set of benchmark exercises will be divided into two or more “threads” of related designs, creating an opportunity to exercise model year upgrades and redesigns within the benchmark process.

Program Structure

Figure 5 illustrates the major components of the overall ARPA RASSP program. Each of the four boxes within the shaded area corresponds to a particular procurement action and to one or more contractors.

The RASSP program is managed by the ARPA Program Manager, who is supported by representatives of each of the Services. All program participants draw upon the existing EDA and DSP industrial infrastructure for independent development and products.

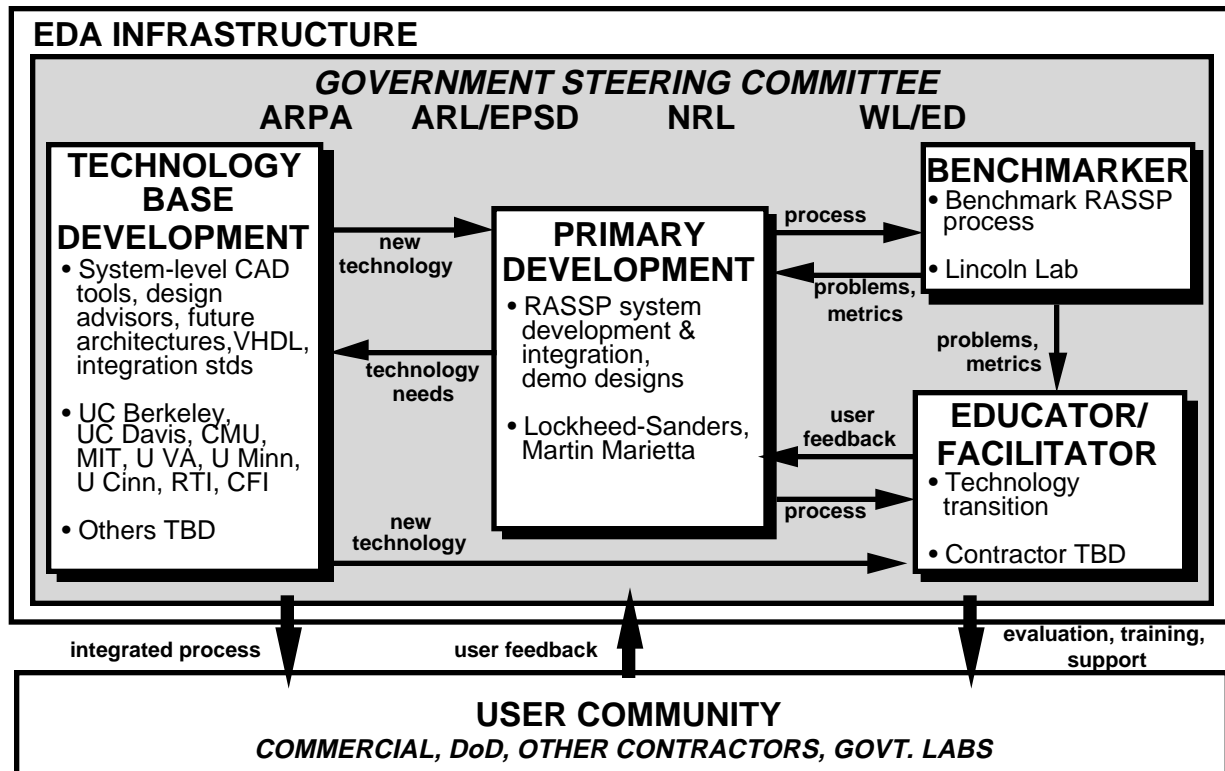


Figure 5. The major components of the RASSP program and their interrelationships.

Primary Development and Demonstration

The primary development contractors are at the center of the RASSP program. They are responsible for development, integration, and demonstration of a comprehensive RASSP design environment. This includes development of a suitable:

- signal processor architecture
- design methodology
- virtual prototyping methodology
- design for testability methodology
- RASSP data base
- cost and "ility" models
- manufacturing interface
- technology insertion plan
- technique for inheriting legacy systems
- business plan

and other tasks as necessary. In addition, the primary development contractor must carry out the semiannual benchmark and system demonstration design exercises.

Teams led by Lockheed Sanders, Inc. (Nashua, NH) and Martin Marietta Advanced Technology Laboratories (Moorestown, NJ) have been selected as primary development contractors. The system demonstration planned by the Lockheed team is an image processor module designed as a pre-planned product improvement (P³I) insertion candidate for the Common Integrated Processor of the F-22 tactical fighter aircraft. The module would provide image processing functions needed to support automatic target recognition using video or forward-looking infrared (FLIR) sensors. The Martin Marietta demonstration is an integrated communication, navigation, and identification (ICNI) module, also designed as an F-22 P³I. Annual releases of their respective RASSP Design Environments are planned by both contractors, nominally in May of each year beginning in 1994.

Technology Base Development

Technology base development contractors are responsible for developing or accelerating specific EDA technologies or standards which can then be used by the primary development contractors, either directly or through adoption into EDA vendor products. The first ten RASSP technology base awards were made to the following organizations:

- CAD Framework Initiative
- Massachusetts Institute of Technology
- University of California, Berkeley
- University of Cincinnati (two awards)
- Carnegie Mellon University
- Research Triangle Institute
- University of California, Davis
- University of Minnesota
- University of Virginia

These awards are for research in the following general areas:

- advanced nonlinear and symbolic algorithms, and their architectural and design implications
- comprehensive system design environment technologies
- development of integration standards for tool interoperability
- tools for development and reuse of software and hardware models

- binary-to-binary real-time object code translation
- VHDL extensions and usage
- estimation of algorithm implementation requirements

A second technology base procurement is currently in progress, and is expected to result in an additional four to eight awards. The areas of interest for the second technology base procurement are generally the same as those given above, but with extra emphasis on VHDL model libraries, built-in test technology, and benchmarking methods for integrated design processes.

Benchmarking

The benchmarking contractor is responsible for designing, administering, and evaluating the series of semiannual design exercises. This contractor is independent of both the primary development and technology base contractors, and is experienced with both embedded signal processor design and DoD applications. The Massachusetts Institute of Technology's Lincoln Laboratory (MIT/LL) was selected for this role.

While MIT/LL must verify compliance of each benchmark design with the specifications, the more important function is to evaluate the design process which created that design. A significant challenge is therefore defining quantifiable metrics for the integrated design process. Still under development at this writing, these metrics are critical to establishing a credible track record which demonstrates rapid and affordable processor development.

Lincoln Laboratory, in cooperation with the ARPA/Tri-Service Steering Committee, has selected a synthetic aperture radar (SAR) image formation processor for an unmanned aerial vehicle (UAV) as the thread for the first series of benchmark exercises. A variety of options are being considered for later benchmarks. For example, development of a commercial-oriented product, instead of a DoD processor, might be emphasized in a second thread of benchmark design exercises.

The Educator/Facilitator

Another important RASSP goal is to ensure that the design environment, methodology, and architectural approaches become adopted by the signal processing community and continue to evolve after the program is completed. The Educator/Facilitator (E/F) contractor plays the leading role in this technology transition process.

The E/F is an independent contractor who serves as a source of knowledge about the RASSP design environment and its performance. The E/F acts as an emissary both among program players and to the broader user and EDA communities. For example, the E/F will maintain an awareness of both ARPA-funded and independent technology base developments relevant to RASSP and assist in technology transition from these efforts to the primary development contractors. The E/F will provide information and technical support services to third party users and vendors concerning benchmark results, establishment of RASSP design capabilities, and training of users through such mechanisms as Mosaic servers, bulletin boards, ftp sites, newsletters, workshops, tutorials, and engineering support services. Another important E/F role is the development of university curricula and learning aids so that RASSP design technology

can be introduced to undergraduate and graduate students. Proposals for the Educator/Facilitator were solicited in December 1993, and this award is expected to be made by Summer 1994. At that time, the RASSP program will be fully underway.

An annual RASSP Conference is planned, with the first in Fall 1994. This conference will provide the most convenient access for the general electronic design community to comprehensive updates on all of the RASSP program developments.