

Processes and Experiences in VHDL Top-Down Design

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Abstract

This paper describes the VHDL related experiences and methods for the RASSP program model year one product. An overview of the "View Concept" is presented first explaining our approach of describing and documenting facets of the RASSP product such as methodology, process, tools, design database, and hardware/network topography. With this concept as a premise, the Virtual Prototype Methodology will be presented addressing specific VHDL models of a digital system from an Algorithmic View down to a Gate View highlighting interactions with the software design methodology and hardware/software codesign. From here the discussion delves into the concept of modeling planes such as physical and logical structure, hierarchy, behavior level of abstraction, and fidelity. The implementation of this methodology to design process building blocks is elaborated showing the dependency on state of the art CAE technologies and highlighting the "Rapid Prototyping Techniques" such as re-use libraries, hardware in the loop simulation, reprogrammable technologies, and hardware emulation.

Specific areas of the methodology will be further discussed in detail drawings from the experiences in Performance Level Modeling, Instruction Set Architecture Modeling, Application Level 2 Modeling, Bus Interface Modeling, and Test Bench Modeling using WAVES. These discussions will encompass engineering practice with the RDE, lessons learned from the DEMO team, and proposed improvements envisioned by the systems engineering team.

In closing, the paper will focus on work ongoing in the areas of emerging VHDL standards like BSDI and WAVES, VHDL related CAE technologies such as cycle based, stream, and timed/untimed domain simulators, and modeling methods such as techniques for multi-threaded operating system VHDL simulators. These closing discussions will relate this ongoing work with specific areas of process improvement for the model year two RASSP product.

Acknowledgment:

The Lockheed Sanders, Inc. RASSP team is under contract to the Naval Research Laboratory, 4555 Overlook Ave., SW, Washington, DC 20375-5326. The Sponsoring Agency is: Advanced Research Projects Agency, Electronic System Technology Office, 3701 North Fairfax Drive, Arlington, VA 22203-1714. The Lockheed RASSP team consists of Lockheed Sanders, Inc., Motorola, Hughes, and ISX.