

INTERFACE DEFINITION SPECIFICATION

FOR THE

BENCHMARK 1 SAR

CONTRACT NO.

CDRL SEQUENCE NO.

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1 Scope

This document applies to the firmware and hardware interfaces for the Benchmark 1 SAR Signal Processor. This is intended to be a working document which will be revised as needed.

1.1 Identification

This Segment Interface Definition Specification applies to the Benchmark 1 SAR.

2 Applicable Documents

2.1 Government Documents

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of the specification, the contents of this specification shall be considered a superseding requirement.

2.1.1 Specifications

N/A

None

2.1.2 Standards

N/A

None

2.1.3 Drawings

N/A

None

2.1.4 Other Publications

N/A

None

Copies of specifications, standards, drawings, and publications required by suppliers in connection with specified procurement functions should be obtained from the contracting agency or as directed by the contracting officer.

2.2 Non-Government Documents

The following documents of the exact issue shown form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of the specification, the contents of this specification shall be considered a superseding requirement.

2.2.1 Specifications

N/A

None

2.2.2 Standards

N/A

None

2.2.3 Drawings

N/A

None

2.2.4 Other Publications

N/A

None

Technical society and technical association specification standards are generally available for reference from libraries. They are also distributed among technical groups and using Federal Agencies.

3 Interface Specifications

This section defines the interfaces within and external to the Benchmark 1 SAR Signal Processor. It is divided into 3 sections. The first is an overview of the high level connectivity. The second defines the internal interfaces. The third section defines the external interfaces.

3.1 Interface Diagrams

The signal processor consists of the following elements:

- a) Data I/O Module
- b) Host Interface Module
- c) Processing Element Module
- d) Control Program Firmware
- e) Signal Processing Firmware

Figure 3–2 shows how these elements are connected both physically and logically.

Figure 3.4–1 shows the hierarchy for the system/segment. Figure 3.4–2 shows a component view of the system/segment.

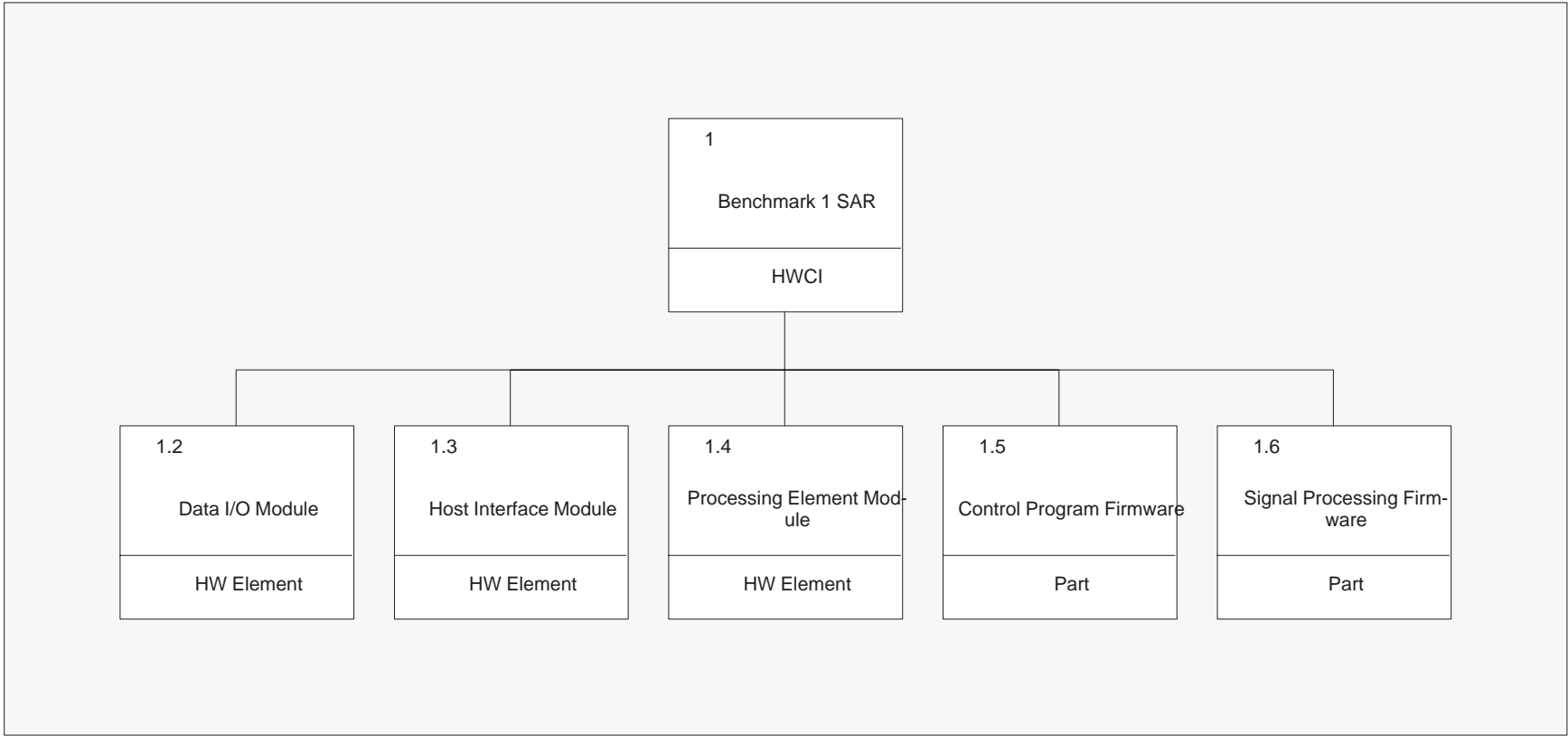


FIGURE 3.1-1. System/Segment Hierarchy

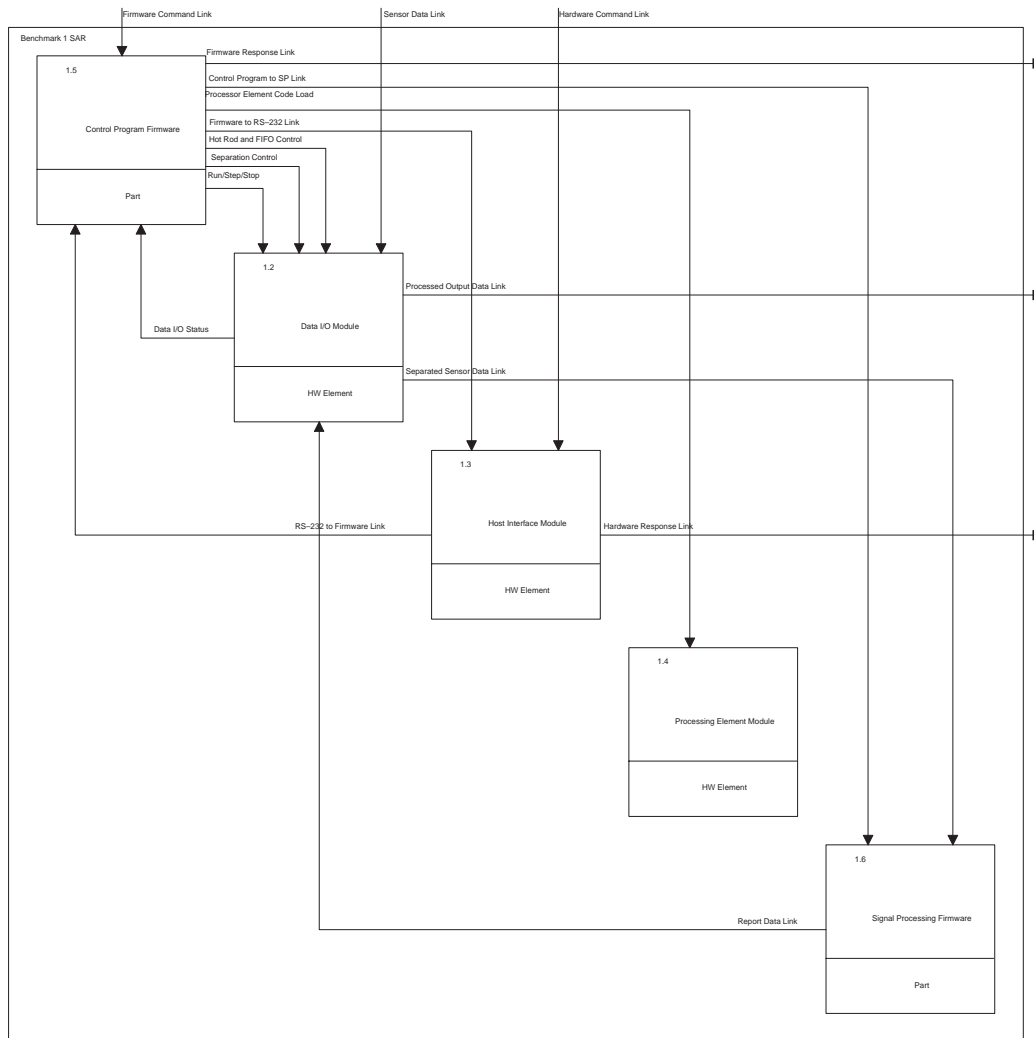


FIGURE 3.1-2. System/Segment Component View

3.2 Internal Interfaces

3.2.1 CP Firmware and Data I/O Module

The CP firmware and Data I/O Module interface is a logical interface which is accessed through the VME bus. The details of this interface are TBD.

The following sections specify the different item links which are contained in this interface.

3.2.1.1 Data I/O Status

The Data I/O Status item link carries the status of the Data I/O Module to the Control Program firmware. This is accessed through the physical VME bus. The specific addresses and bit positions

are indicated in the following paragraphs.

3.2.1.1.1 FIFO Status

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.1.2 HR Error

This is a five bit field consisting of a single bit for each polarization and one bit for non-polarization errors. These bits when high indicates that an error has been detected on the fiber optic interface during the reception of the indicated polarization. A bit will go high when an error is detected and reset after TBD. The method for reading this bit is TBD. The Hot Rod asserts an error if one (or more) of the nibbles is received as an invalid 5-bit symbol. Since "Error" is generated on a word-by-word basis, the following action decisions are built into the Data I/O Board:

1. Set the data sample values to "0" whenever a word is received in error.
2. Set a status bit to the "error" condition whenever an error is detected for any sample in a range pulse.
3. If the error occurs in the range pulse that is used for the AUX data, use the AUX data from the next valid range pulse (or continue to use the previous value).
4. If the error occurs in an input sample during the Barker Code or any other non-PRI data. The fifth error bit shall be set.
5. Need to set some other error status bit if the error rate exceeds some threshold.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.2 Hot Rod Control

The Hot Rod Control item link is a logical link from the Control Program to the Data I/O module which carries the Controls for the Hot Rod module. This item link is established through the VME bus. The specific details are TBD.

3.2.1.2.1 FIFO Control

Access Characteristics:

Bus : VME

Address : TBD
Bit Position : TBD

3.2.1.2.2 HR Control

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.2.3 HR Receive Divide Control

This item is a 2 bit control which selects the receive data rate of the Hot Rod module. These shall always be set to [1 0]. The method for setting these bits is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.2.4 HR Receive Loop Open

This control is a single bit which controls the receive input for the Hot Rod Module. If this bit is set [1], the module is in the loop back mode which selects the loop back port for input instead of the fiber port. If this bit is cleared [0], the data is received over the fiber interface. The method of controlling this bit is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.2.5 HR Transmit Divide Control

This item is a 2 bit control which selects the transmit data rate of the Hot Rod module. These shall always be set to [1 0]. The method for setting these bits is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.2.6 HR Transmit Loop Open

This control is a single bit which controls the transmit output for the Hot Rod Module. If this bit is set [1], the module is in the loop back mode which sends all the output data to the loop back port for input instead of the fiber port. If this bit is cleared [0], the data is sent over the fiber interface. The method of controlling this bit is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.3 Run/Step/Stop

The Run/Step/Stop link is a logical link from the Control Program to the Data I/O Module. Which carries the Run/Stop/Step control and the Number of Steps parameter. The physical layer of this interface is the VME bus. The specifics of this link are TBD.

3.2.1.3.1 Number of Steps

This item controls the number of PRIs which the Data I/O Module will process. The format and method for loading this value is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.3.2 Run/Stop/Step

This item allows the Control Program Firmware to change the state of the Data I/O Module. The Data I/O Module controls the processing by either running continuously, running for a fixed number of PRIs, or stop at the end of the current PRI. The method for transferring this control item is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.4 Separation Control

The Separation Control link is a logical link from the Control Program to the Data I/O module which carries the information required to separate and process the received PRI data. The physical layer of this link is the VME bus. The specifics of this link are TBD.

3.2.1.4.1 FIR Parameters

The FIR Parameters data set is a combination of both the odd and even FIR Filter Weights.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.4.2 Processed Polarizations

This item is the control for the Data I/O module which indicates the polarizations to be processed. The format and method for loading this information is TBD.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.4.3 Stored Even Filter Weights

This data item is a set of 48 real FIR filter coefficients used for the raw even data. This data set will be padded with zeros on the end if less than 48 coefficients are used.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.1.4.4 Stored Odd Filter Weights

This data item is a set of 48 real FIR filter coefficients used for the raw odd data. This data set will be padded with zeros on the end if less than 48 coefficients are used.

Access Characteristics:

Bus : VME

Address : TBD
Bit Position : TBD

3.2.2 CP Firmware and Host Interface Module

The CP firmware and Host Interface Module interface is a logical interface which is used to access the Host Interface hardware. Other than serving as a platform for the CP firmware, the host interface also provides an RS-232 serial interface.

The following sections specify the different item links which are contained in this interface.

3.2.2.1 Firmware to RS-232 Link

The Firmware to RS-232 Link is used to connect the Control Program Firmware to the outgoing RS-232 interface. The specifics are TBD.

3.2.2.1.1 Echoed Characters

This item is a copy of each character received over the RS-232 interface. As a character is processed, it is echoed back over the RS-232 interface.

3.2.2.1.2 Response Message

This item is any message sent from the Control Program Firmware to the host through the RS-232 interface. This message will be in ASCII. The actual mechanics of sending the data are TBD.

3.2.2.1.3 RS-232 Control

This item is the set of controls for the RS-232 interface on the Host Interface Module. This set of controls is TBD.

3.2.2.2 RS-232 to Firmware Link

The RS-232 to Firmware Link is used to connect the Control Program Firmware to the incoming RS-232 interface. The specifics are TBD.

3.2.2.2.1 Command Line Characters

These items are the individual characters received over the RS-232 interface. The method for reading these characters is TBD.

3.2.2.2.2 RS-232 Status

This item is the set of status indicators for the RS-232 interface on the Host Interface Module

3.2.3 Firmware Interface

The Firmware Interface is a logical interface between the Control Program Firmware and the Signal Processing Firmware. The details of this interface are TBD.

The following sections specify the different item links which are contained in this interface.

3.2.3.1 Control Program to SP Link

The Control Program to SP link is a logical link from the Control Program to the Signal Processing firmware which carries the information required to process the received PRI data. The physical layer of this link is the VME bus. The specifics of this link are TBD.

3.2.3.1.1 Processed Polarization

This data item indicates which polarization is being processed by this functional chain. As indicated in Section 3.2, the functionality of the firmware element must be repeated once for each of the processed polarizations.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.3.1.2 Processing Parameters

The Processing Parameters data set is a combination of the Equalization Weights, RCS Weights, and Reference Kernels.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.4 Processor Element Code Load

The Processor Element Code interface is a logical interface from the Control Program Firmware to the Processor Element Module hardware. It carries the Signal Processing firmware executable to the hardware. The full details are TBD.

The following sections specify the different item links which are contained in this interface.

3.2.4.1 Processor Element Code Load

The Processor Element Code Load item link is a logical link from the Control Program to the Processor Element module. This link loads the executable image for the Signal Processing firmware from the Host Interface Module to the Processor Element Module. The physical layer of this interface

is the VME bus. The specific details of the interface are TBD.

3.2.4.1.1 Signal Processing Firmware Executable

This item is the executable code for the Signal Processing Firmware. It is stored on the Host Interface Module and the Control Program must load the firmware in each Processor Element Module. The method for loading this code is TBD.

3.2.5 RACEway

The RACEway is an adjunct physical interface to the VME interface. It is defined in VITA 5–1994. The following sections specify the different item links which are contained in this interface.

3.2.6 SP Firmware and Data I/O Module

The SP firmware and Data I/O Module interface is a logical interface which is accessed through the RACEway. The details of this interface are TBD.

The following sections specify the different item links which are contained in this interface.

3.2.6.1 Report Data Link

The Report Data Link is a logical link from the Signal Processing firmware to the Data I/O module.

This link carries the processed output data for a frame to the Data I/O Module. The physical layer of this interface is the RACEway. The specific details are TBD.

3.2.6.1.1 Frame Report Data

This data item is the data which will be included in the Processed Data Output. It shall have the format indicated below.

Frame Report Data Format

Word	Bits 31:16	Bits 15:00
1	Polarization Code	Polarization Code
2–58	Aux Word 1–57	Aux Word 1–57
59	I Pixel Value: Range 0, Azimuth 0	
60	Q Pixel Value: Range 0, Azimuth 0	
...	...	
1081	I Pixel Value: Range 0, Azimuth 511	
1082	Q Pixel Value: Range 0, Azimuth 511	
1083	I Pixel Value: Range 1, Azimuth 0	
1084	Q Pixel Value: Range 1, Azimuth 0	
...	...	
2096187	I Pixel Value: Range 2047, Azimuth 511	
2096188	Q Pixel Value: Range 2047, Azimuth 511	

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.6.2 Separated Sensor Data Link

The Separated Sensor Data Link is a logical data link which carries PRI data and Aux data from the Data I/O Module to the Signal Processing firmware. The physical layer of this link is the RACEway. The specifics of this link are TBD.

3.2.6.2.1 Aux Data

This data item is the set of 57 Auxillary Data words which were received with the 256th PRI of the current Frame. Each of these words is 16 bits wide. Table ?? indicates the data in each of the words.

Table ??		Auxillary Data Word Definition
Word	# Words	Contents
1	2	INS North Position
3	2	INS East Position
5	1	INS Down Position
6	1	Level North Velocity
7	1	Level East Velocity
8	2	Motion Sensed North Position
10	2	Motion Sensed East Position
12	2	Motion Sensed DOWn Position
14	2	Motion Sensed North Velocity
16	2	Motion Sensed East Velocity
18	2	Motion Sensed Down Velocity
20	2	Aimpoint North Position
22	2	Aimpoint East Position
24	2	Aimpoint Down Position
26	1	Time WOrd #1
27	1	Time WOrd #2
28	2	Range to Aimpoint
30	2	Velocity Toward Aimpoint
32	1	ANtenna Yaw Command
33	1	Antenna Pitch Command
34	1	Antenna Roll Command
35	1	Antenna Status Flag
36	1	Scanner Position
37	1	Range to DME7
38	1	Reserved
39	1	Reserved
40	2	Avg. North Update for INS
42	2	Avg. East Update for INS
44	1	MoComp Freq. Coef.
45	1	MoComp Phase Coef
46	1	Azimuth Prefilter Coef.
47	1	Heading Angle
48	1	Pitch Angle
49	1	Roll Angle
50	1	Radar Mode
51	1	Time in msec
52	1	IMU x velocity
53	1	IMU y Velocity
54	1	IMU z Velocity

55	1	IMU Neg. Head. Ang. Rate
56	1	IMU Neg. Roll Ang. Rate
57	1	IMU Neg. Pitch Ang. Rate

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.6.2.2 Integer I/Q Baseband Data

This data item contains $2032 - N$ complex (I/Q) baseband data samples where N is the number of taps used in the FIR filters. This data is in TBD (24 bit integer) format.

Access Characteristics:

Bus : VME
Address : TBD
Bit Position : TBD

3.2.7 VME Backplane

The VME backplane is a standard 32 bit VME bus which conforms to TBD.

The following sections specify the different item links which are contained in this interface.

TBD

3.3 External Interfaces

3.3.1 Control and Diagnostics Interface

The Control and Diagnostics Interface is used to control the operation of the SAR Signal Processor. This interface is an RS-232 interface where the SAR-SP is configured as a TBD. The data transfer is to have the following characteristics:

Baud Rate : 9600, 19200, 38400*
Data Bits : TBD
Start Bits : TBD
Stop Bits : TBD
Parfity : TBD

The following sections specify the different item links which are contained in this interface.

3.3.1.1 Hardware Command Link

The communications protical of the Command Link is found under the Control and Diagnostic Interface description.

3.3.1.1.1 Control Data

The Control Data consists of character strings used for the Commands listed in Table 7 of the RASSP Benchmark 1 Technical Description.

3.3.1.2 Hardware Response Link

The communications protocol of the Response Link is found under the Control and Diagnostic Interface description.

3.3.1.2.1 Diagnostics Data

The Diagnostics Data consists of character strings used in response to the Commands listed in Table 7 of the RASSP Benchmark 1 Technical Description.

3.3.2 Data Interface

The Data Interface carries sensor input data to the SAR-SP and processed data from the SAR-SP. This interface is a fiber optic interface which is the equivalent of the 'Hot Rod' interface module. The following sections specify the different item links which are contained in this interface.

3.3.2.1 Processed Output Data Link

The protocol for the Processed Output Data Link is found under the Data Interface description.

3.3.2.1.1 Processed Output Data

The Processed Output Data is the fully formatted frame reports from the Signal Processor to the outside world. Bits 38 and 39 of each word in the report contain the 2 bit polarization code for the frame (0-HH, 1-HV, 2-VH, 3-VV). The format of bits 31 through 0 is

Word	31:16	15:00
1-5	zeros	zeros
6-18	Barker Code	Barker Code
19-20	Unused	Unused
21	Polarization Code	Polarization Code
22-78	Aux Data	Aux Data (repeated)
79	I Pixel Value ; Range 0, Azimuth 0	
80	Q Pixel Value ; Range 0, Azimuth 0	
81	I Pixel Value ; Range 0, Azimuth 1	
82	Q Pixel Value ; Range 0, Azimuth 1	
...	...	
2097229	I Pixel Value ; Range 2047, Azimuth 511	
2097230	Q Pixel Value ; Range 2047, Azimuth 511	

3.3.2.2 Sensor Data Link

The protocol for the Sensor Data Link is found under the Data Interface description.

3.3.2.2.1 Sensor Data

The Sensor data is the data received from the outside world over the fiber optic interface. Each PRI contains a frame for each polarization in the order HH, HV, VH, VV. This data contain 40 bit words. Bits 0 through 2, 17, 18, and 33 through 39 of the word are unused. The format of bits 0 through 32 of a single frame is:

Words	32	31:20		19	16	15:04		03
1–5	0	Unused		0	0	Unused		0
6–18	B	"		B	B	"		B
19–20	F	"		F	F	"		F
21–36	H	Odd Samples		H	H	Even Samples		H
37–	A	"		A	A	"		A
2052	A	"		A	A	"		A
2053–	Filler Words (variable number)							

B – Barker Code, F – Filler Bits, H – Header, A – Aux Data

3.3.3 Firmware Outside World Interface

The Firmware/Outside World interface is the logical interface between the Control Program Firmware and the ADTS or outside world. It corresponds to the physical RS–232 interface. It carries command characters and response messages.

The following sections specify the different item links which are contained in this interface.

3.3.3.1 Firmware Command Link

The Firmware Command Link is the logical link for the incoming RS–232 character stream.

3.3.3.1.1 Control Data

The Control Data consists of character strings used for the Commands listed in Table 7 of the RASSP Benchmark 1 Technical Description.

3.3.3.2 Firmware Response Link

The Firmware Response Link is the logical link for the outgoing RS–232 character stream.

3.3.3.2.1 Diagnostics Data

The Diagnostics Data consists of character strings used in response to the Commands listed in Table 7 of the RASSP Benchmark 1 Technical Description.

TBD

4 Notes

4.1 Acronyms and Abbreviations

TBD – To Be Determined

5 UN-RESOLVED AND OPEN ISSUES