

Can we stop the growing disparity between the potential of IBIS model parameters and the reality of delivered model parameters ?

SIEMENS

Agenda



Missing IO-Models with different PVT



Missing IBIS parameters



IBIS QUALITY



IBIS work in progress (WIP)



Summary

SIEMENS

E.Lenski / Com SC SL CE23 IBIS Summit DATE 2005 11. March 2005

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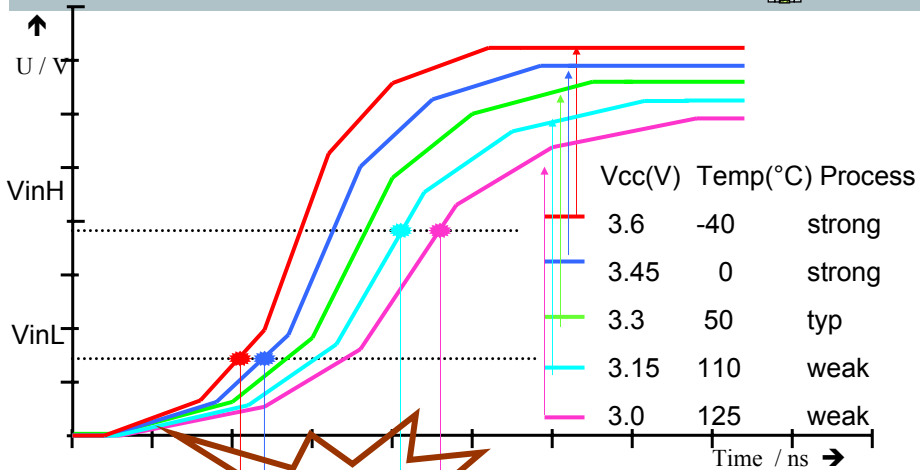
PVT model classes



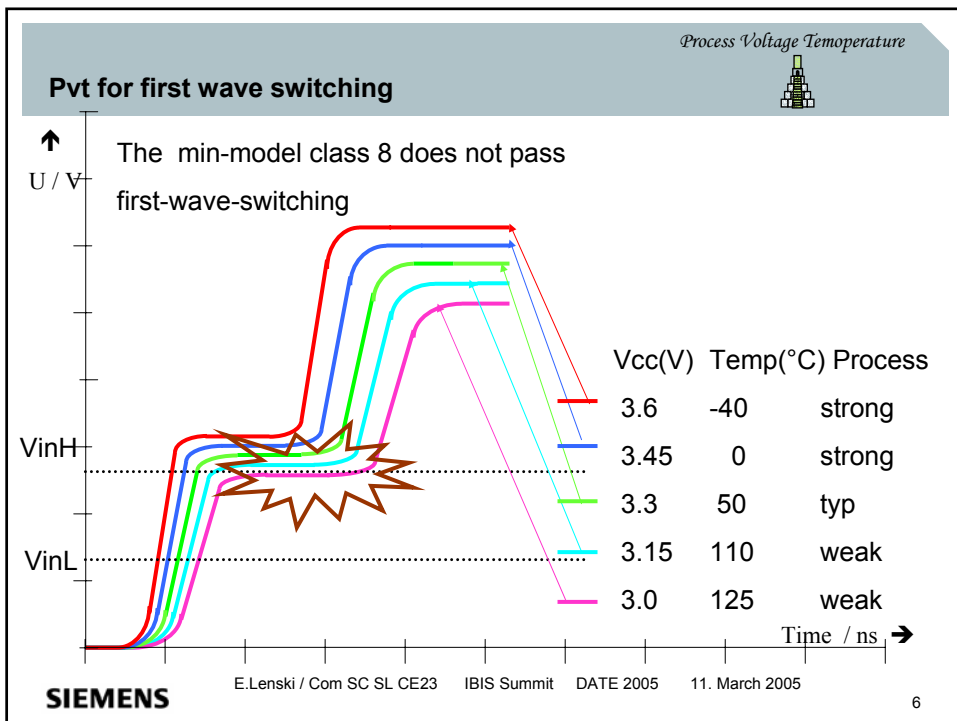
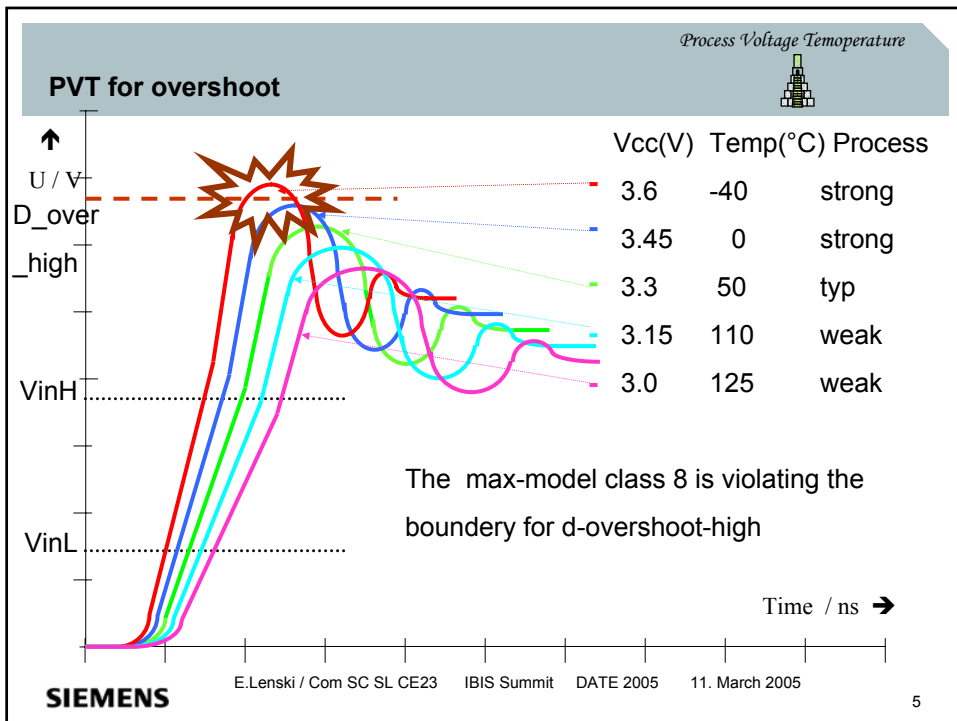
Model class	δV_{cc}	T_j	Process	Vcc(V)	Temp(°C)	Process
1	$\pm 5\%$	0 – 110	$\pm 2\sigma$	3.6	-40	strong
2	$\pm 5\%$	0 – 110	$\pm 3\sigma$	3.45	0	strong
3	$\pm 5\%$	m40 – 125	$\pm 2\sigma$	3.3	50	typ
4	$\pm 5\%$	m40 – 125	$\pm 3\sigma$	3.15	110	weak
5	$\pm 10\%$	0 – 110	$\pm 2\sigma$	3.0	125	weak
6	$\pm 10\%$	0 – 110	$\pm 3\sigma$			
7	$\pm 10\%$	m40 – 125	$\pm 2\sigma$			
8	$\pm 10\%$	m40 – 125	$\pm 3\sigma$			

$\pm 2\sigma$ means 95,5% of all shipped parts fulfill these limits
 $\pm 3\sigma$ means 99,7% of all shipped parts fulfill these limits
 $\delta V_{cc} \pm 5\%$ means e.g. 3P3V -- 3P15V -- 3P45V
 $\delta V_{cc} \pm 10\%$ means e.g. 3P3V -- 3P00V -- 3P60V

PVT for prop-delay



Different Tpd :





PVT for HCMOS and SSTL

- HCMOS : Vcc : 2.0V - 6.0V
- LVCMOS : Vcc : 1.0V - 5.5V
- SSTL2 : Vcc: 2.3V - 2.7V

Example 1 LVCMOS

- Vcctyp : 1.2V LVCMOS12
- 2.5V LVCMOS25
- 3.3V LVCMOS33
- 5.0V LVCMOS5

Example 2 SSTL2 / DDR:

- DDR200-333 : Vcc : 2.3V - 2.7V
- DDR400 : Vcc : 2.5V - 2.7V

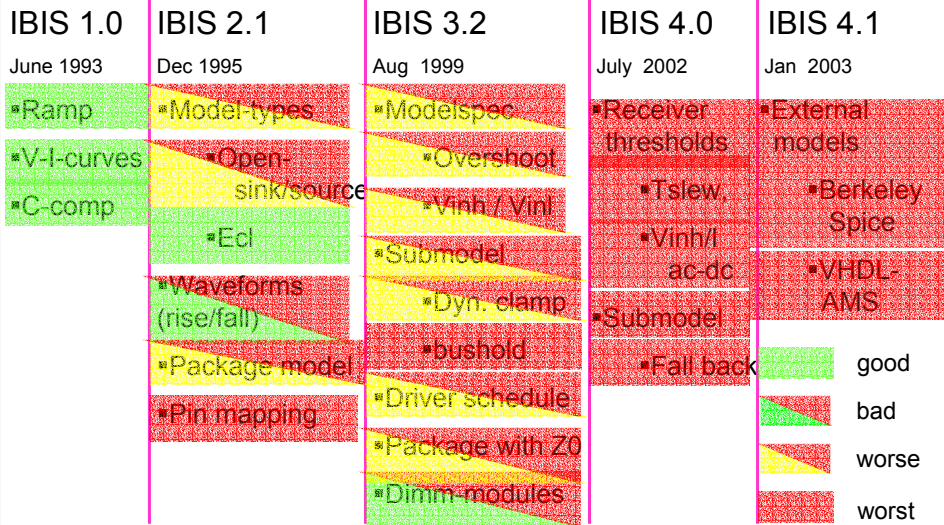
Some vendors supply these IO-models for logic devices



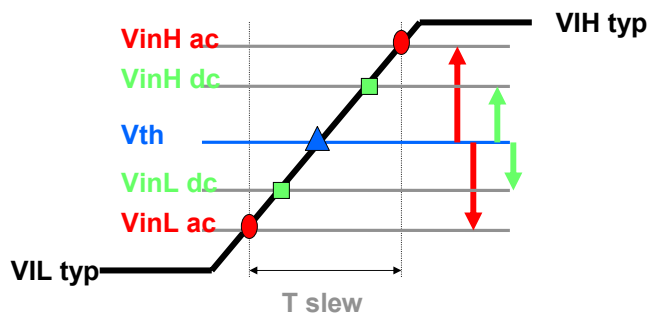
History of 'important' IBIS keywords/parameters

IBIS 1.0	IBIS 2.1	IBIS 3.2	IBIS 4.0	IBIS 4.1
June 1993	Dec 1995	Aug 1999	July 2002	Jan 2003
<ul style="list-style-type: none"> ▪Ramp ▪V-I-curves ▪C-comp 	<ul style="list-style-type: none"> ▪Model-types <ul style="list-style-type: none"> ▪Open-sink/source ▪Ecl ▪Waveforms (rise/fall) ▪Package model ▪Pin mapping 	<ul style="list-style-type: none"> ▪Modelspec <ul style="list-style-type: none"> ▪Overshoot ▪Vinh / Vinl ▪Submodel <ul style="list-style-type: none"> ▪Dyn. clamp ▪bushold ▪Driver schedule ▪Package with Z0 ▪Dimm-modules 	<ul style="list-style-type: none"> ▪Receiver thresholds <ul style="list-style-type: none"> ▪Tslew, ▪Vinh/I ac-dc ▪Submodel <ul style="list-style-type: none"> ▪Fall back 	<ul style="list-style-type: none"> ▪External models <ul style="list-style-type: none"> ▪Berkeley Spice ▪VHDL-AMS

Support of ,important' IBIS keywords/parameters

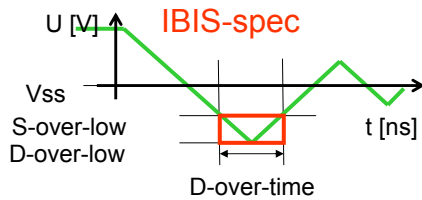


SSTL / Receiver thresholds missing





Overshoot missing



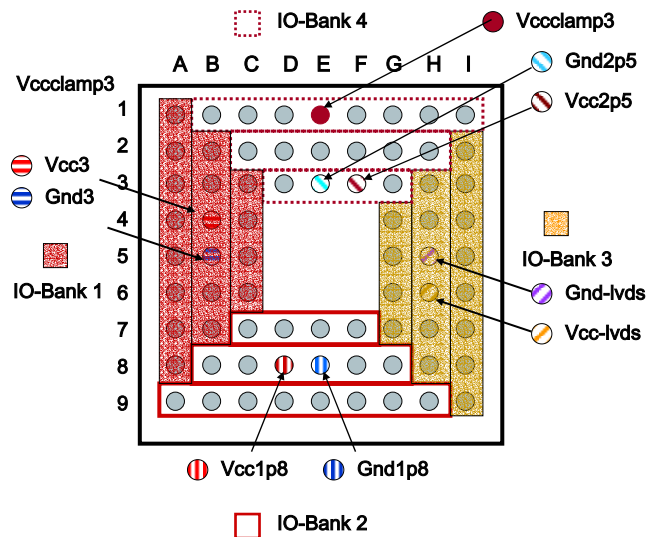
Philips supply these parameters for logic devices

[S_overshoot_low]	-0.52V	-0.60V	-0.65V
[S_overshoot_high]	4.05V	3.88V	4.33V
[D_overshoot_low]	-1.20V	-1.47V	-1.11V
[D_overshoot_high]	4.44V	4.53V	4.77V
[D_overshoot_time]	3ns	3ns	3ns



Pin mapping missing

- A1 GND3 VCC3
/ 3P3V-Signalpin
- B1 GND2p5 VCC2p5 NC
/ 2P5V-Signalpin with diode
/ to 3P3V
- B4 NC VCC3
/ 3P3V supply
- B5 GND3 NC
/ Gnd for 3P3V
- E1 NC VCCclamp3
/ VCCclamp3P3V supply
- H4 GND-lvds VCC-lvds
- H6 NC VCC-lvds
- I1 GND2p5 VCC2p5





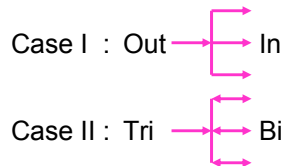
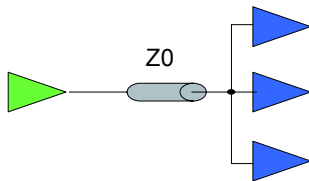
IO-Model-type not correct



IBIS-IO-Model type

- Input
- Output
- 3-state
- I/O

Example : mismatch DB - IBIS



Which will be the correct driver in case II ?



IBIS Quality documents

- IQ_checklist_kit.zip
 - IQ-checklist.xls
 - IQ-specification.txt
 - USING-IQ-checklist.ppt
- IQ_example.ibs
 - An example of an IBIS file that was run through the checklist



Current status of IQ Committee Work

- Checklist is complete
- Checklist kit is complete
- Example is available
- Detailed instructions are available
- Current task : list of additional checks that could be added to Golden Parser
- Wanted: engineers / volunteers who will use the checklist and provide feedback



Specifications for IBIS-IO-models



www.eigroup.org/ibis/ibis.html

IBIS spec

Cookbook (new release will cover up to IBIS4.0)

Accuraccy spec

Quality spec



ICM Spec



Not yet supported by the tools, but:

- It will/must be a standard
- Can be changed into another format (for the tools)
- Information about connector / package available in a specified format



Missing descriptions for

- driver schedule models
gtlp with open-sink/source (→ new cookbook)
totem-pole-multistages
- Fall back submodels
- ODT-models (dynamic clamp) (→ new cookbook)
- Bushold submodels
- Keyword ReceiverThresholds (SSTL)



ICEM and bird95



ICEM

- Integrated circuit electrical model for description of the power activities of the whole IC, especially for the core
- For EMI- predictions
- For ICEM there is a cookbook available



Bird95.1

- Description of the current behavior of the outstage and their prestages with the use of I-T-tables
- For SSO- analysis
- Supply of a good cookbook required

Summary (work to do to decrease the disparity)



Models with different PVT must be delivered (possible in IBIS) for new models



Quality Checklist is ready for use by vendors (it's for free)



Important keywords/parameters for new models must be supported by the vendors



IBIS supports different possibilities to help the vendors to create IBIS-models with the newest keywords/parameters



For new keywords, the ibis-forum must provide a clear description / cookbook