VIP-TSC Standardization Update

Accellera VIP-TSC has made significant progress in 2009. The VIP-TSC outlined two phases to its work. We completed part of the first phase by releasing the Recommended Guidelines for Interoperability between VMM and OVM in June 2009 that can be downloaded at http://www.accellera.org/activities/vip/VIP_1.0.pdf. The committee continues progress to complete and release the accompanying interoperability kit that can be used by popular verification platforms.

The committee has recently addressed its second phase to deliver a standard verification methodology and common base class library (CBCL) to enable users to deploy an efficient, reusable, and interoperable SystemVerilog verification environment. In the last quarter more than a dozen presentations were made to collect the requirements for creating such a methodology. The presenters represented leading user companies, IP providers, services providers, and EDA vendors.

On December 16, 2009, a comprehensive proposal for development of a Universal Verification Methodology (UVM) was made. The goal of the proposal is to create a UVM that combines best of OVM and VMM as well as other contributions. The committee initiated a vote in 7 parts that concluded on December 23, 2009 with the following motions being passed:

- A specification document will be created which details the API of the CBCL. This specification document will include the methodologies for the CBCL usage. The converged reference CBCL will be developed by the Accellera VIP TSC.
- The development of this converged reference CBCL will be recommended an Accellera flagship project for at least the next three years.
- The name of the CBCL, the specification document, and API will be the “Universal Verification Methodology” and will use the acronym “UVM”.
- The OVM version 2.0.3 will be used as the starting point for the UVM.
- Complementary functionality from the VMM, OVM releases and/or other contributions from Accellera VIP TSC members may be incorporated into the UVM subject to the vote of the Accellera VIP TSC.
- The goal of the Accellera VIP TSC is to have the first cut release of the UVM done by Q1’10.
- The development model detailed in Intel’s foil posted on December 16, 2009 http://www.accellera.org/apps/org/workgroup/vip/download.php/2007/Intel%20CBCL%20work%20model%20and%20process%20final.ppt will be used as the foundation for UVM development with the understanding that logistics and details will be refined and altered as needed.

Accellera will drive development of the UVM specification, a reference implementation, and API targeting an early beta release of UVM 1.0 by Q1’10

The committee’s development process is now being refined to address many logistical details that must be managed to support a smooth and unencumbered development and release process for the UVM.

We thank all the participants for their contributions so far and look forward to their continued participation, support, and cooperation. If you would like to monitor the work of the group or become

an active member, please visit http://www.accellera.org/activities/vip to see how you can become involved.

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