
Three-Conductor Modeling of Power/Ground Noise

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Motivation

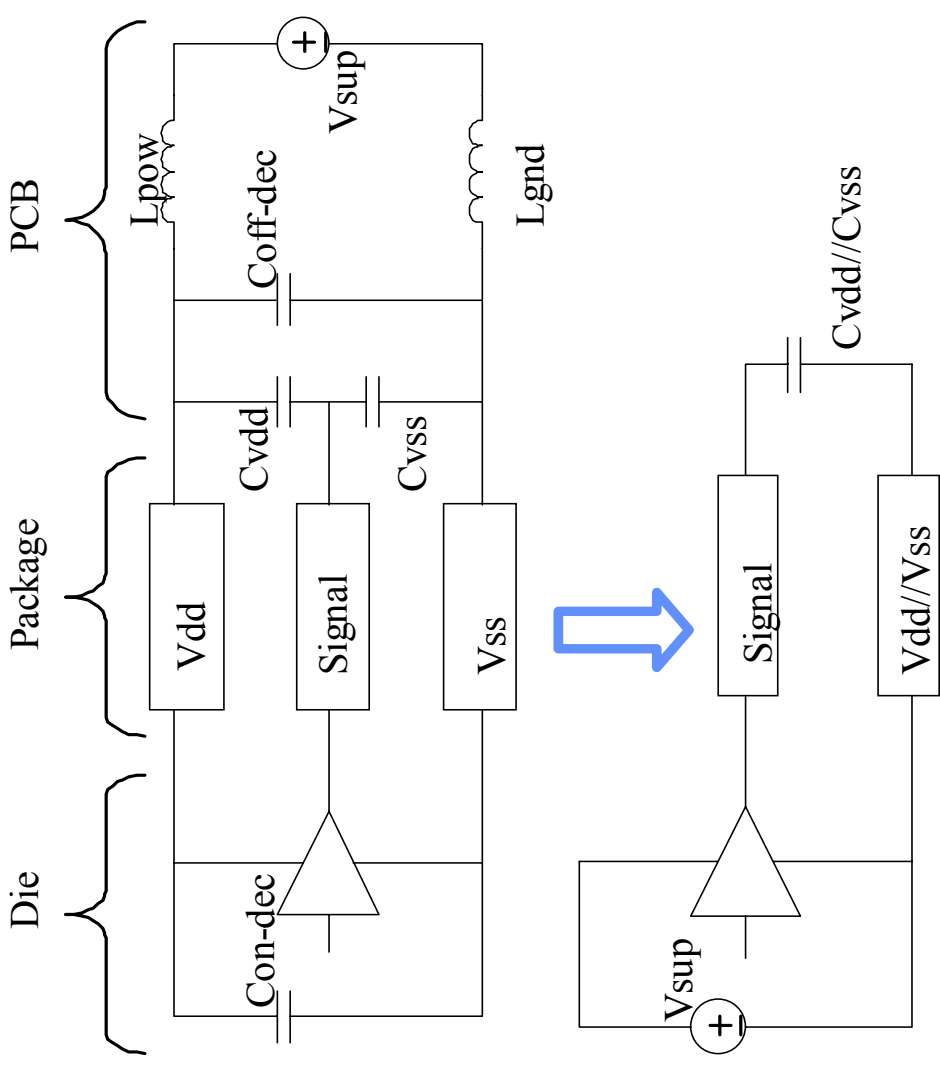
- ❑ Investigation of the interaction between switching I/O drivers and the power/ground noise in chip packages
- ❑ Three-conductor model is ...
 - a model that includes the power and ground lines separately in addition to the signal lines
- ❑ Three-conductor model can ...
 - be used to optimize IC package layer allocation, decoupling capacitor placement, distribution of supply wirebonds, BGA balls, etc.
 - model SSN, return path discontinuities, etc.



2-Conductor vs. 3-Conductor Models

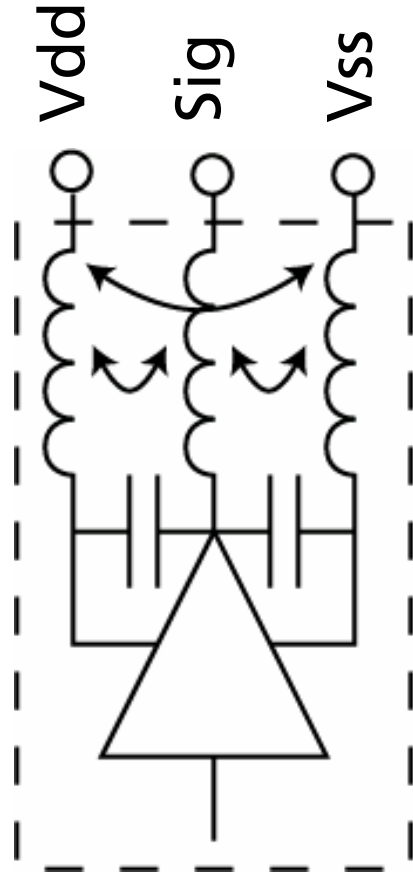
- ❑ 3-conductor model can account for correct current return paths
 - Power supply perturbations

- ❑ 2-conductor model assumes perfect decoupling
 - Vdd is AC short-circuited with Vss
 - Ideal power supply distribution



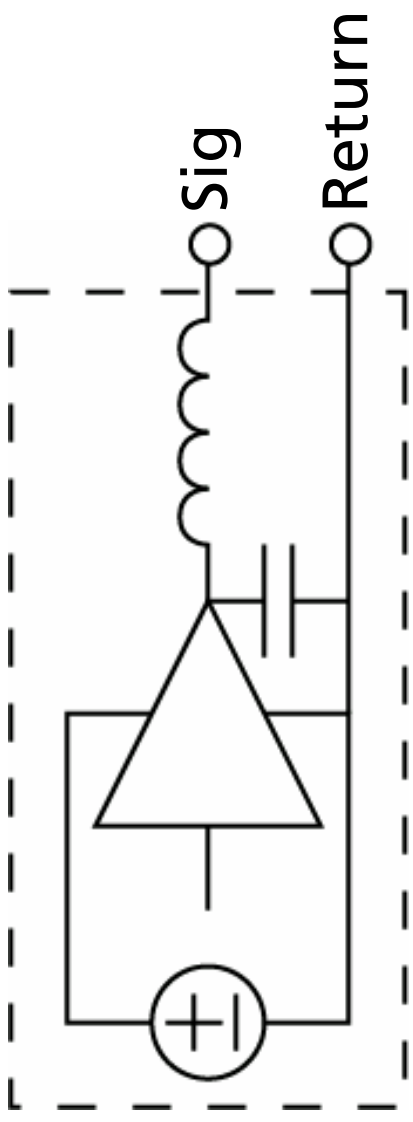
IBIS Issues

- ❑ Pin Mapping is needed to associate each I/O buffer with its corresponding supply bus
- ❑ Parasitics on the power supply distribution has to be included in the package model
- ❑ C_Comp has to be distributed between power and ground
- ❑ Power/Gnd Simulation: <http://www.eda.org/pub/ibis/summits/sep01/raghuram.pdf>
- ❑ SSN: <http://www.eda.org/pub/ibis/summits/jan00/unger.zip>



3- Conductor Model

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2- Conductor Model



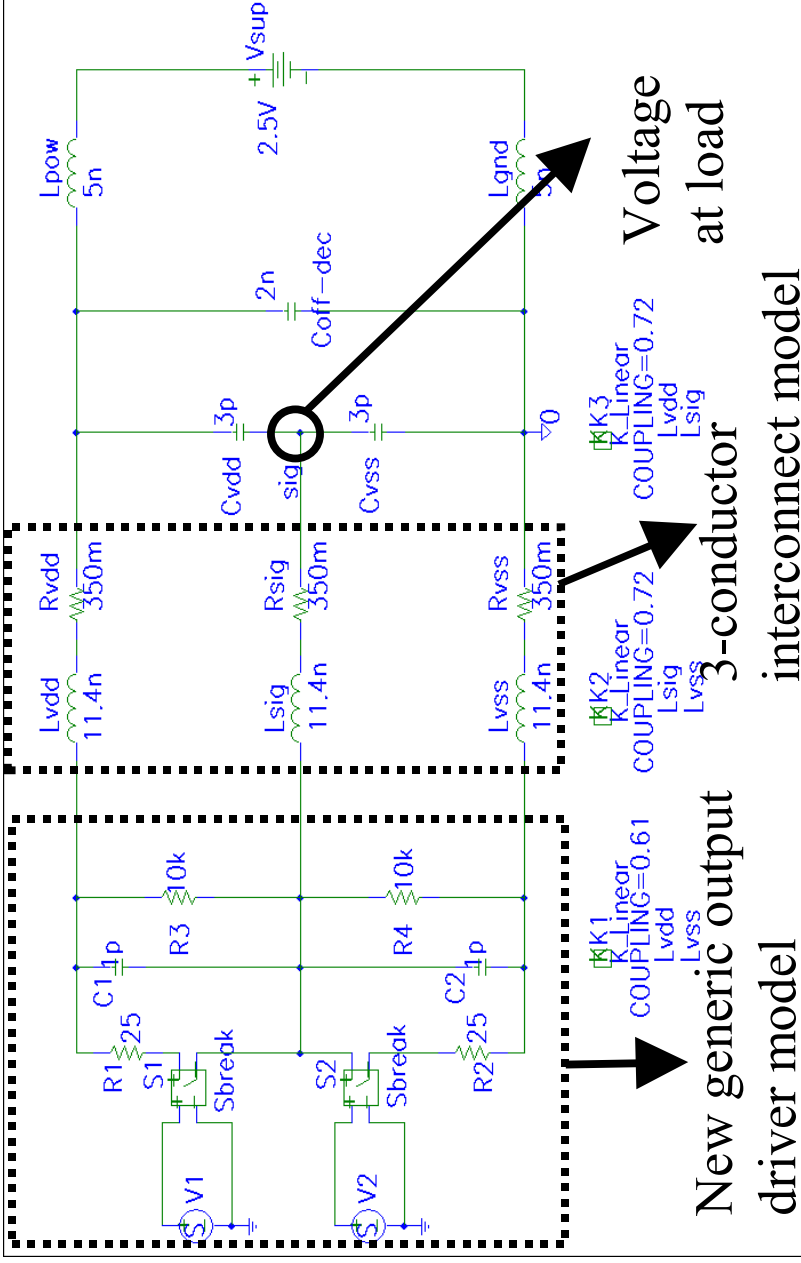
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PHILIPS

3-Conductor Spice Model

- ❑ Output driver model:
 - Rise and fall times, period, on-resistances for pull-up and pull-down
- ❑ 3-conductor interconnect:
 - Coplanar strips

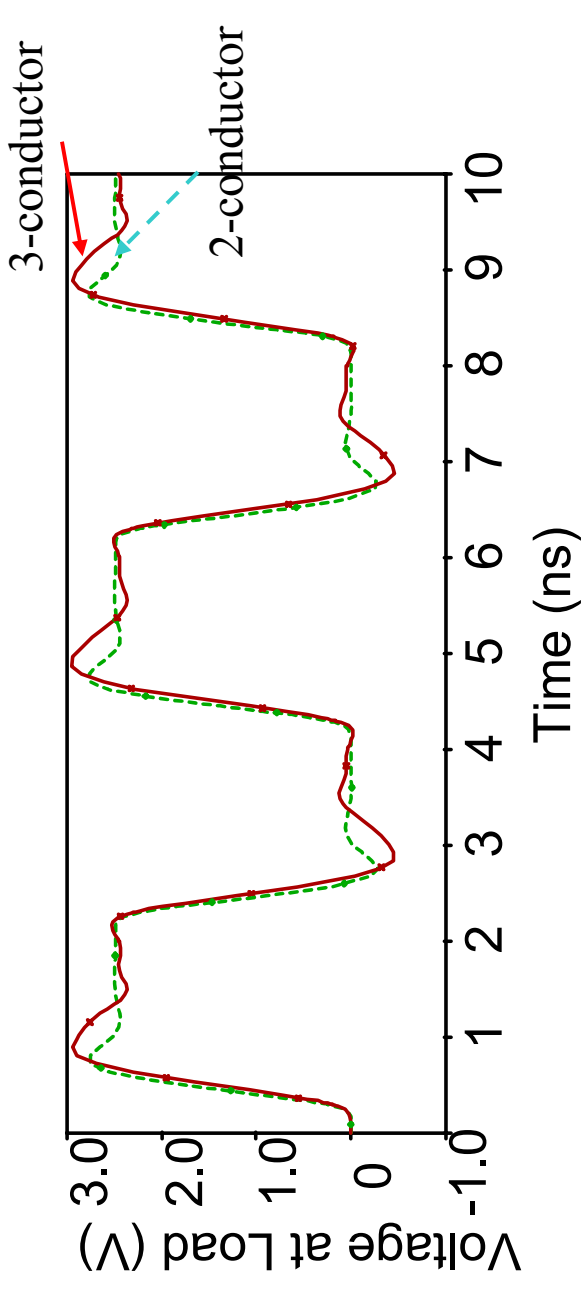


❑ Ref: <http://www.insa-tlse.fr/~emccompo/FinalEngin.pdf>



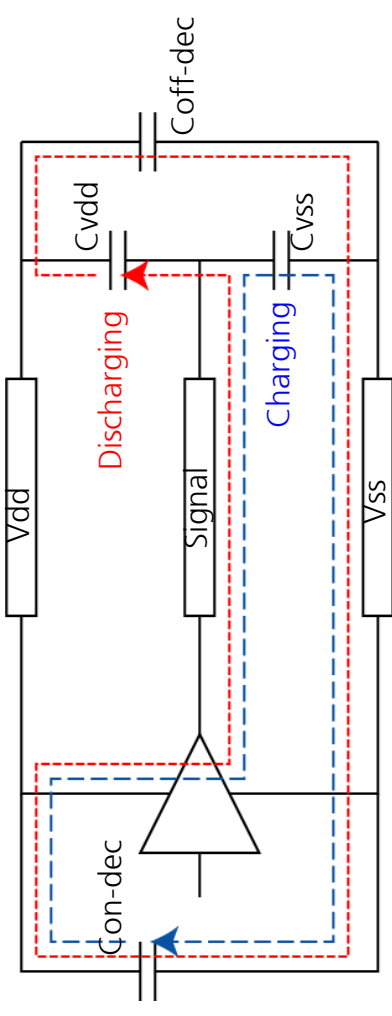
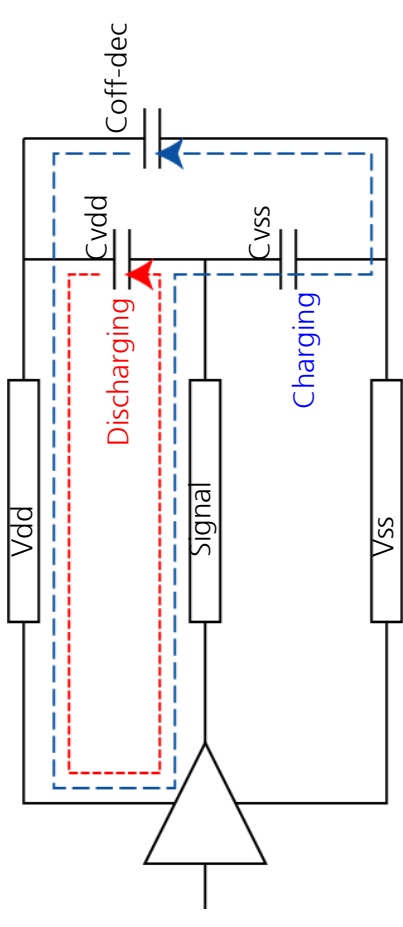
Comparing the 2-Conductor Model with the 3-Conductor Model

- ❑ A 2-conductor model can be obtained by maintaining constant supply voltage
- ❑ => Connect an ideal big enough capacitor or an ideal voltage source at the driver



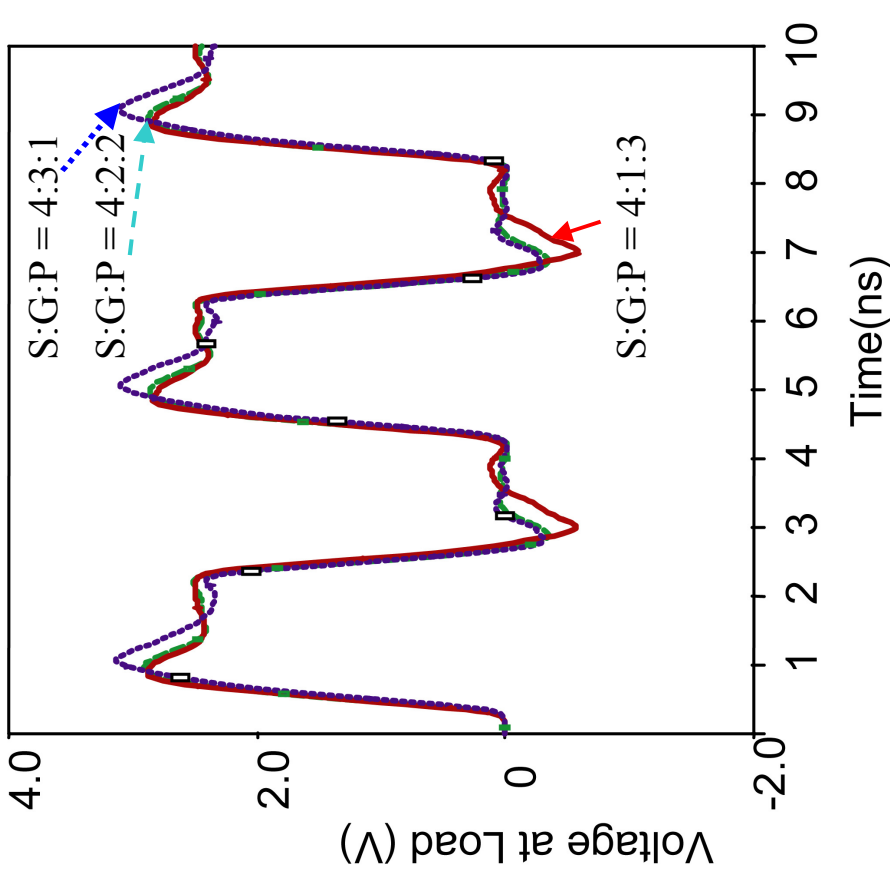
Current Loops at a Low-to-High Transition

- ❑ Con-dec supplies additional current return paths, thereby reducing the impedance seen by the return current
- ❑ Analogue current loops at a High-to-Low transition



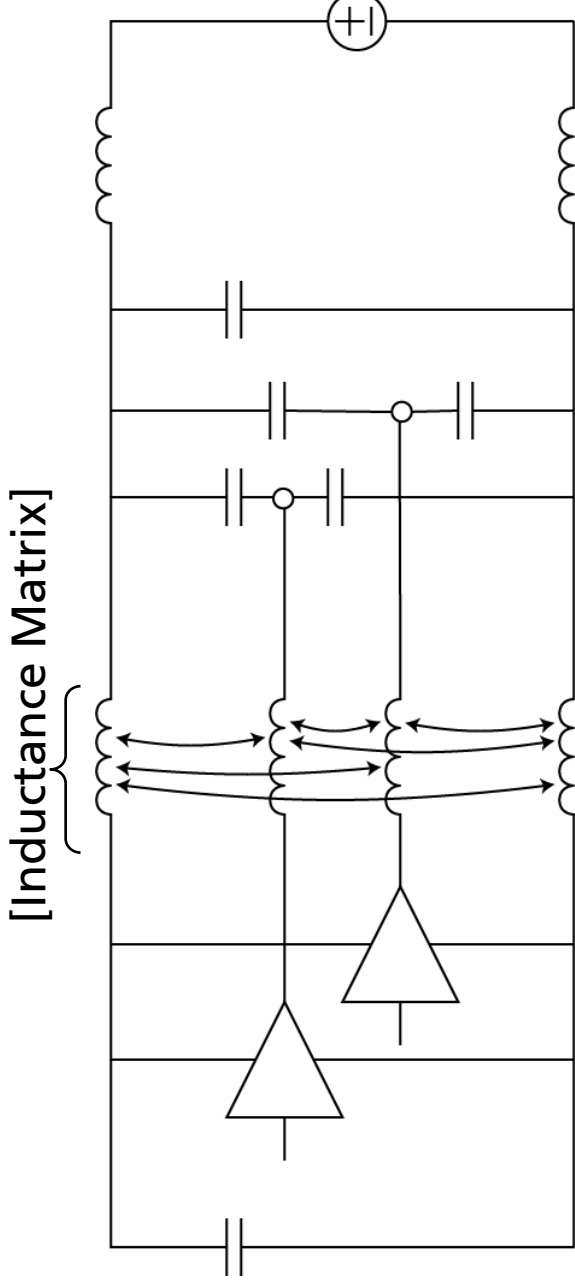
Assignment of Supply Wirebonds

- Low-to-High transition
 - Return path is mainly on the power line
- High-to-Low transition
 - Return path is mainly on the ground line
- An even assignment of supply wirebonds to power and ground gives an optimum signal quality



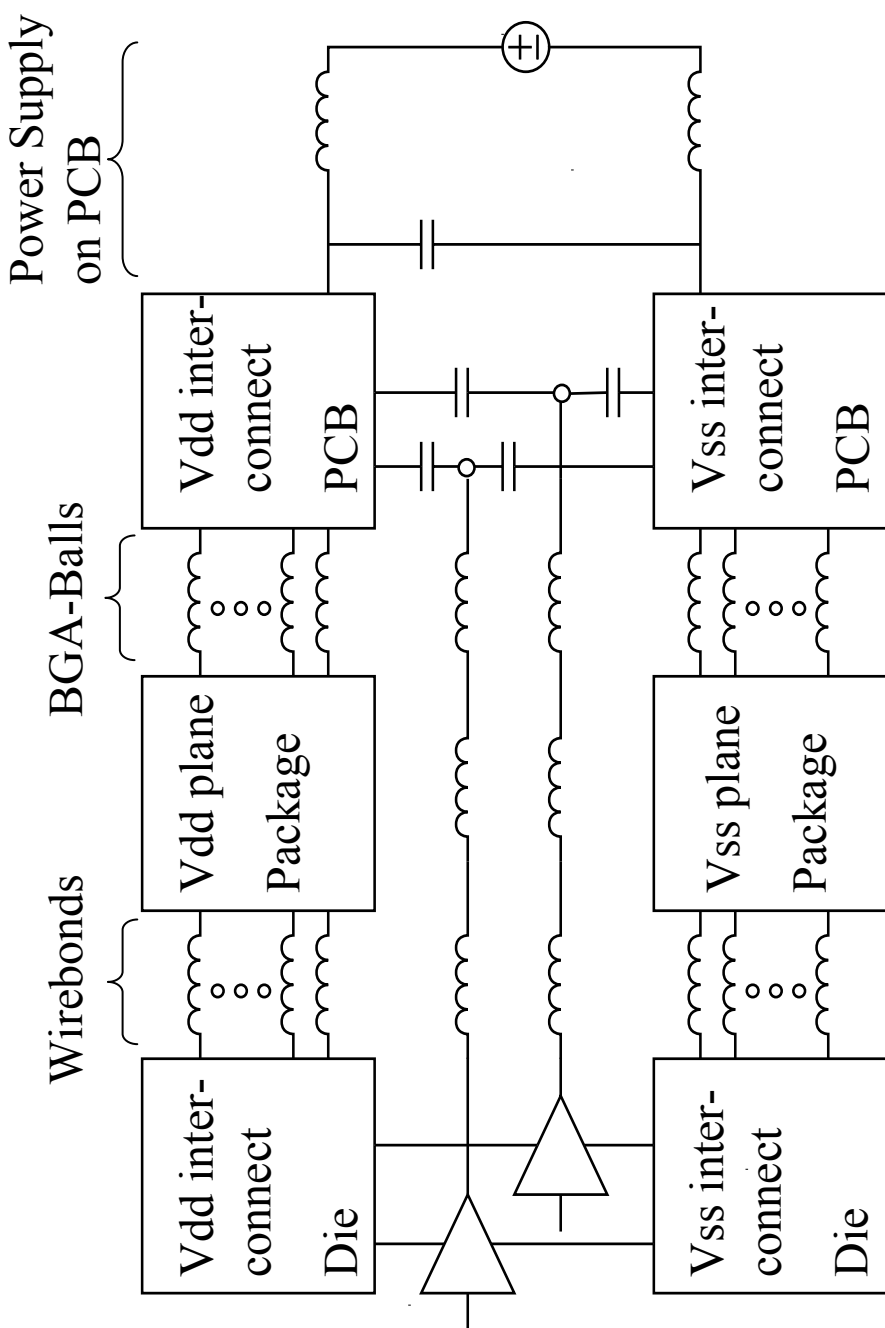
Basic SSN Model

- ❑ SSN can be modeled using the 3 conductor model for multiple pins
- ❑ The partial inductances/resistances can be entered in an IBIS model using the [Inductance/Resistance Matrix] keyword



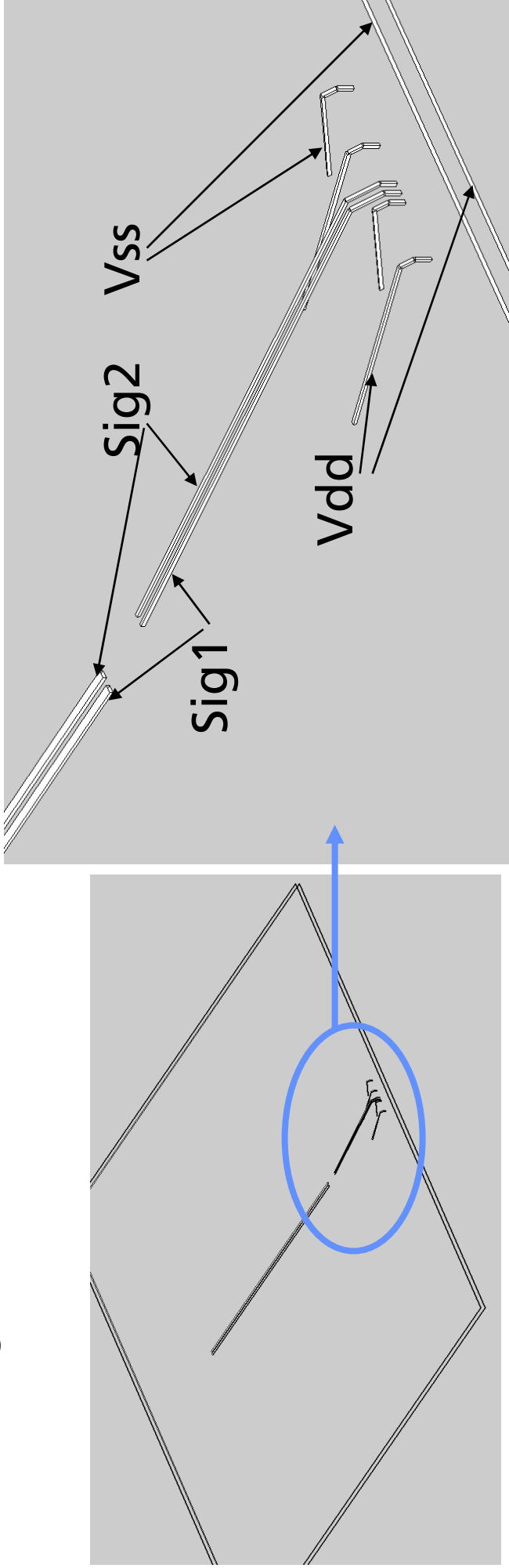
Extended SSN Model

- The voltages and currents at the inner terminals of the package can be observed
- All inductors are coupled (not shown in the figure)
- Modeling of the package planes is not straightforward
- Can be reduced to the basic SSN model if the inner terminals are not of interest
- Cannot be put into IBIS/ICM format due to the coupling between blocks



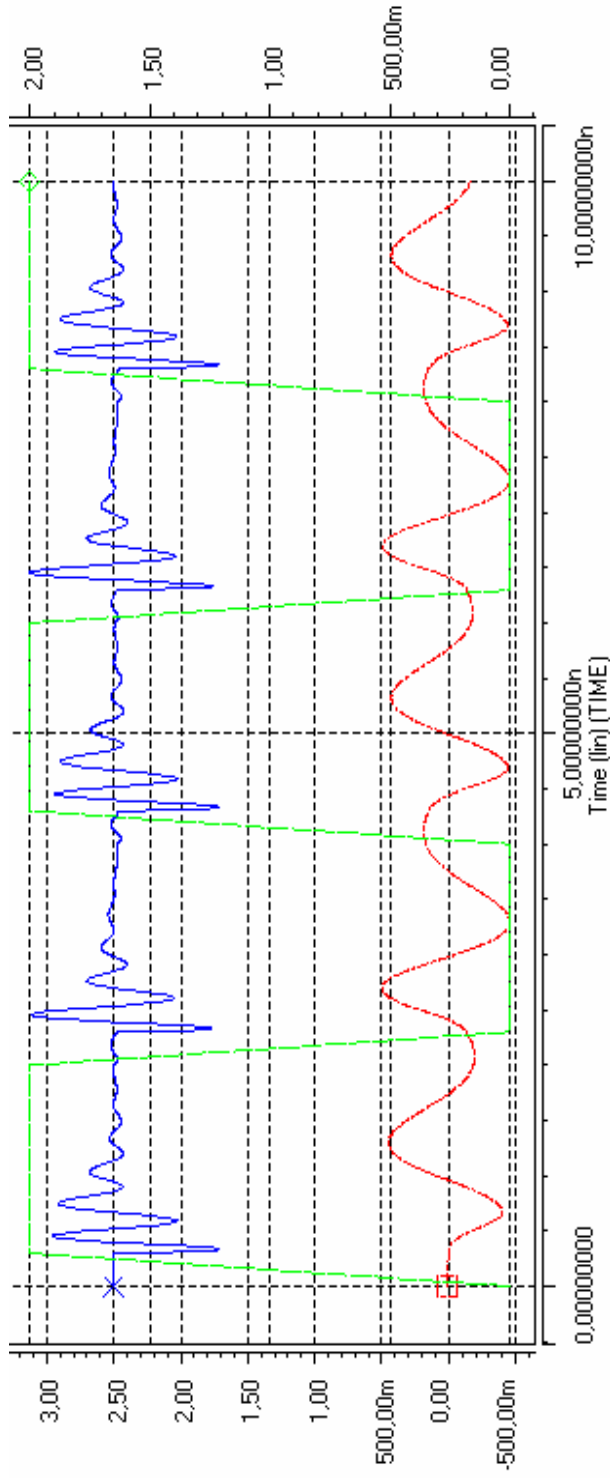
Electrical Model Extraction

- Wirebonds and traces are ideally shorted
- BGA balls neglected
- Trace length: 1cm



Simulation of the Basic SSN Model

- First driver is low (L), second driver is active (X)
- Vrcv**: Quiet line noise at the receiver side
- Vsup**: Voltage fluctuation between Vdd and Vss at the die side
- Vsti**: Stimulus to the second driver



Conclusions

- ❑ 3- Conductor modeling is necessary to account for the interaction between switching I/O drivers and the power/ground noise
 - More information on the accuracy of IBIS models under non-ideal power supply conditions would be helpful
- ❑ Package modeling
 - A proper modeling of the planes is necessary to implement the extended SSN model

