



# *M $\pi$ log*, Macromodeling via Parametric Identification of Logic Gates

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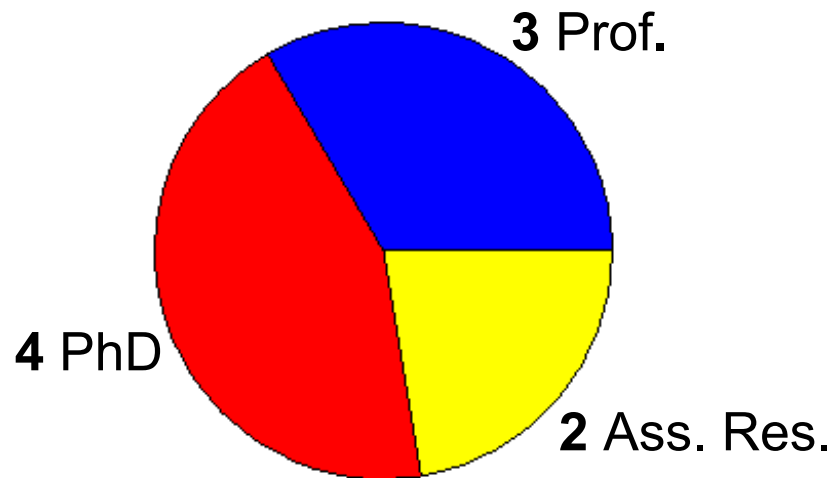
<http://www.eln.polito.it/research/emc>





# EMC Group @ POLITO

## Staff



## Research

Modeling of devices, interconnects and discontinuities in high-speed information and communication systems.

Collaborations:

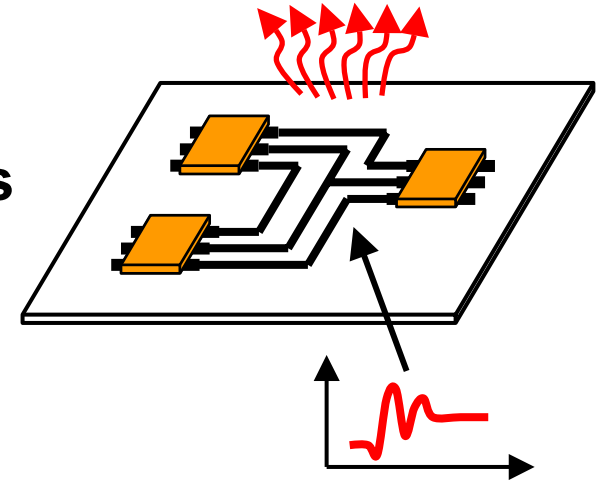
- IBM (USA+GE)
- INTEL (USA)
- CST (GE)



# Background

## High Performance simulation requirements

- Very accurate timing
- Power-supply voltage variation effects
- Temperature effects



- Transistor-level models are not affordable (computation + structure disclosure)
- *Classic* IBIS models not always adequate

→ Complementary Approach

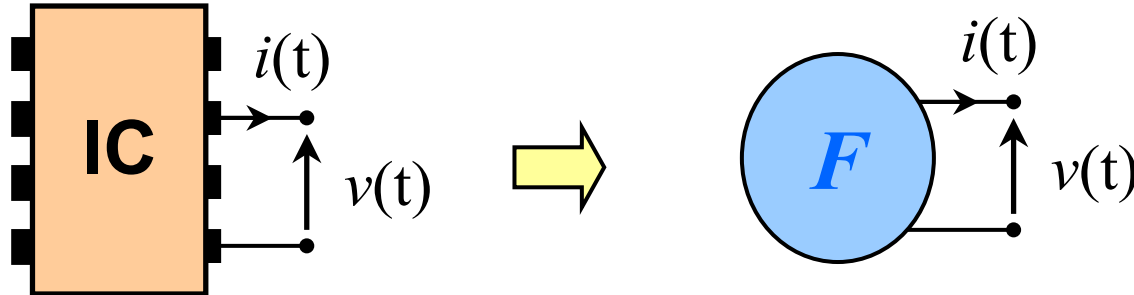


# *Mπlog (i)*

## Macromodeling via Parametric Identification ( $\pi$ ) of Logic Gates

### What is it ?

A mathematical expression reproducing the electrical behavior of the device



$$i = F(v, d/dt)$$

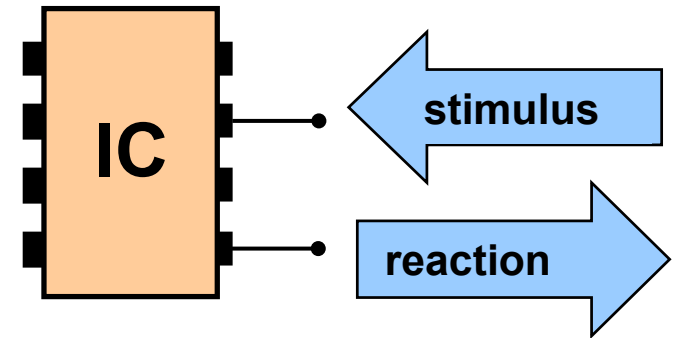
Nonlinear dynamic relationship



# *Mπlog* (ii)

## How does it work ?

- Real Device (or its physical model) is conveniently **stimulated**
- **Reaction** (port transient responses) is used to build the model



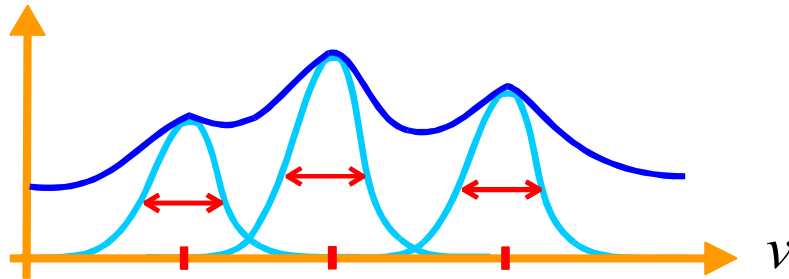


# $M\pi log$ : what is the output ?

**Model structure:**  $F$  is a  $\Sigma$  nonlinear Gaussian Radial Basis Functions (RBF)

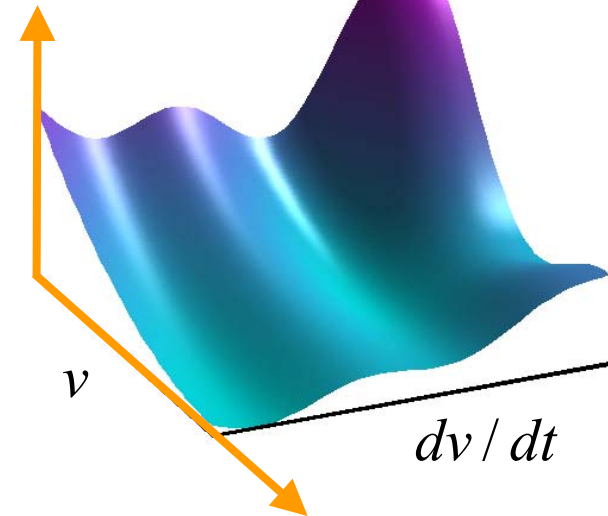
e.g., 
$$i = -a_1 \exp\{-v^2/a_2\} + a_3 \exp\{-(dv/dt)^2\}$$

$F(v, dv/dt)$



unknown parameters: **amplitude, position, spreading**

$F(v, dv/dt)$



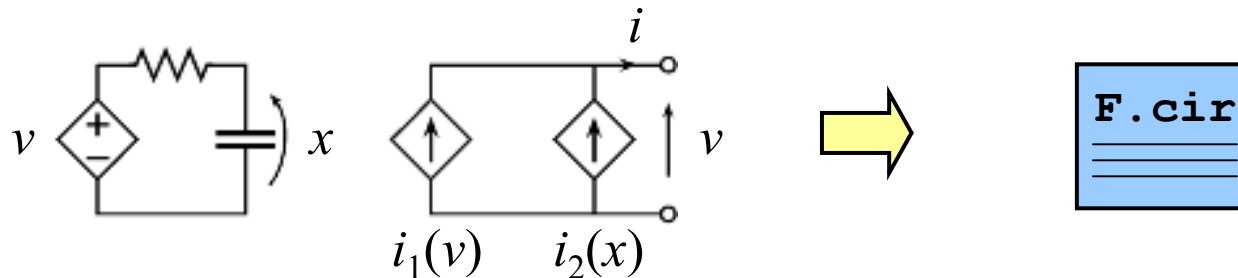


# $\mathbf{M}\pi\mathbf{log}$ : implementation

$$i = -a_1 \exp\{-v^2/a_2\} + a_3 \exp\{-(dv/dt)^2\}$$

**(a) DIRECT EQUATION DESCRIPTION/IMPLEMENTATION**

**(b) CIRCUIT INTERPRETATION & SPICE IMPLEMENTATION**



**(Compatible with IBIS MULTI-LINGUAL Model Support, BIRD #75.8)**



# $M\pi$ log applications

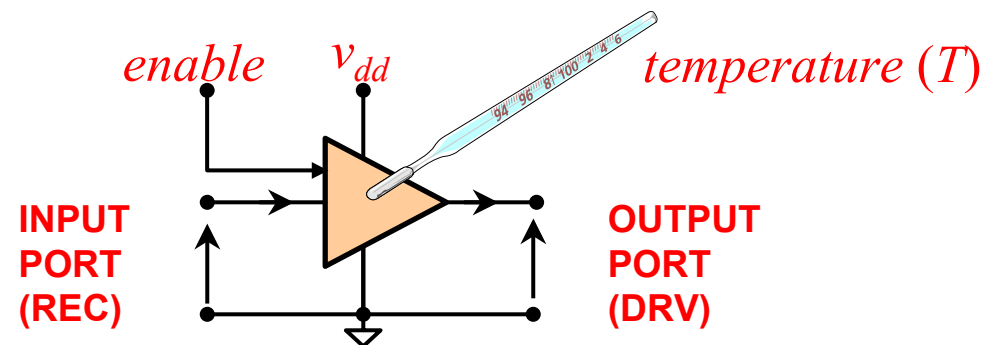
- **Basic macromodels** of Input and Output ports

[I.S.Stievano, F.G.Canavero, I.A.Maio, “Parametric Macromodels of Digital I/O Ports,”  
IEEE Trans. on Advanced Packaging, Vol. 25, No. 2, pp. 255-264, May 2002]

- Inclusion of slowly-varying **device parameters** (eg, **temperature**)
- Inclusion of the **power-supply voltage** variation
- models of the **power supply port**
- models of **tristate drivers**

[I.S.Stievano, F.G.Canavero, I.A.Maio, “ $M\pi$ log,” Proc. Of the 4th Annual IBM CAS  
Conference, Austin, TX, Feb. 21, 2003]

Following examples are based  
on a high-speed IBM CMOS  
transceiver ( $V_{dd} = 1.8$  V)

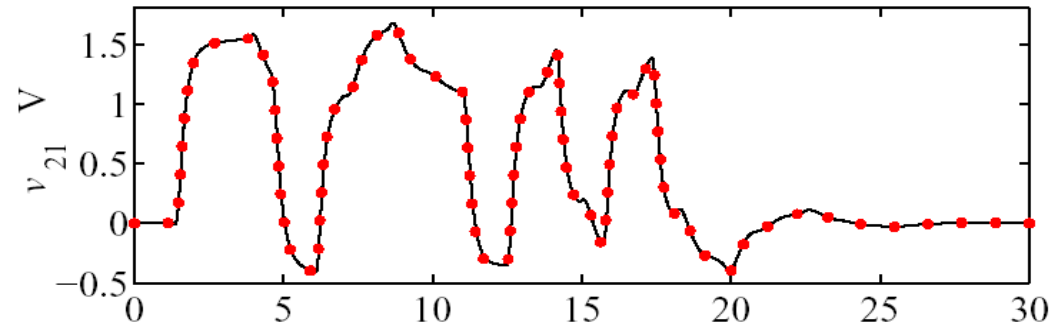
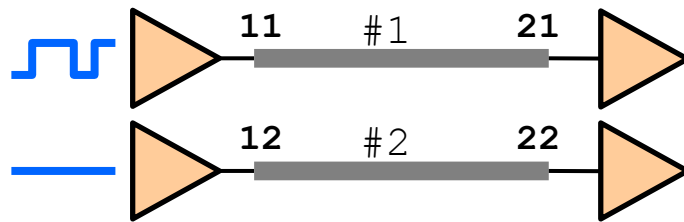




# Example #1: basic devices

High-speed interconnection system with (Z-Series) IBM I/O ports

## Setup

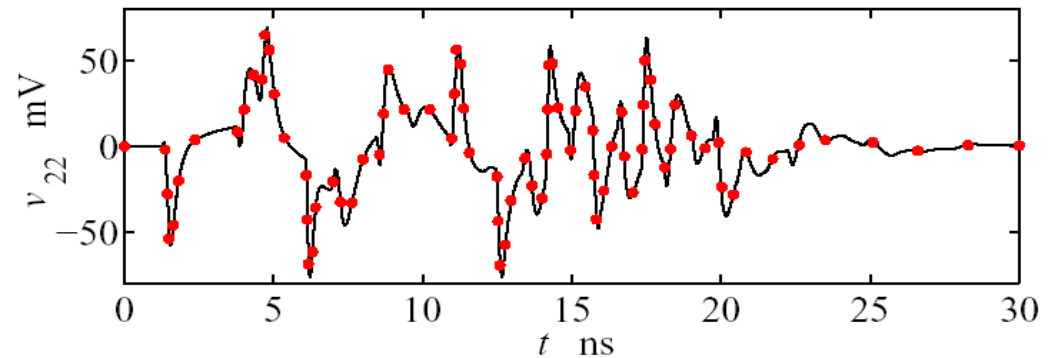


## Models

- Reference (transistor-level)
- **Macromodels (*Mπlog*)**

### CPU TIME (PowerSPICE)

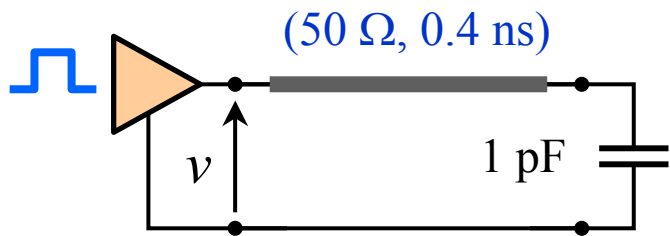
Transistor-level	6 min
<i>Mπlog</i> model	5 s





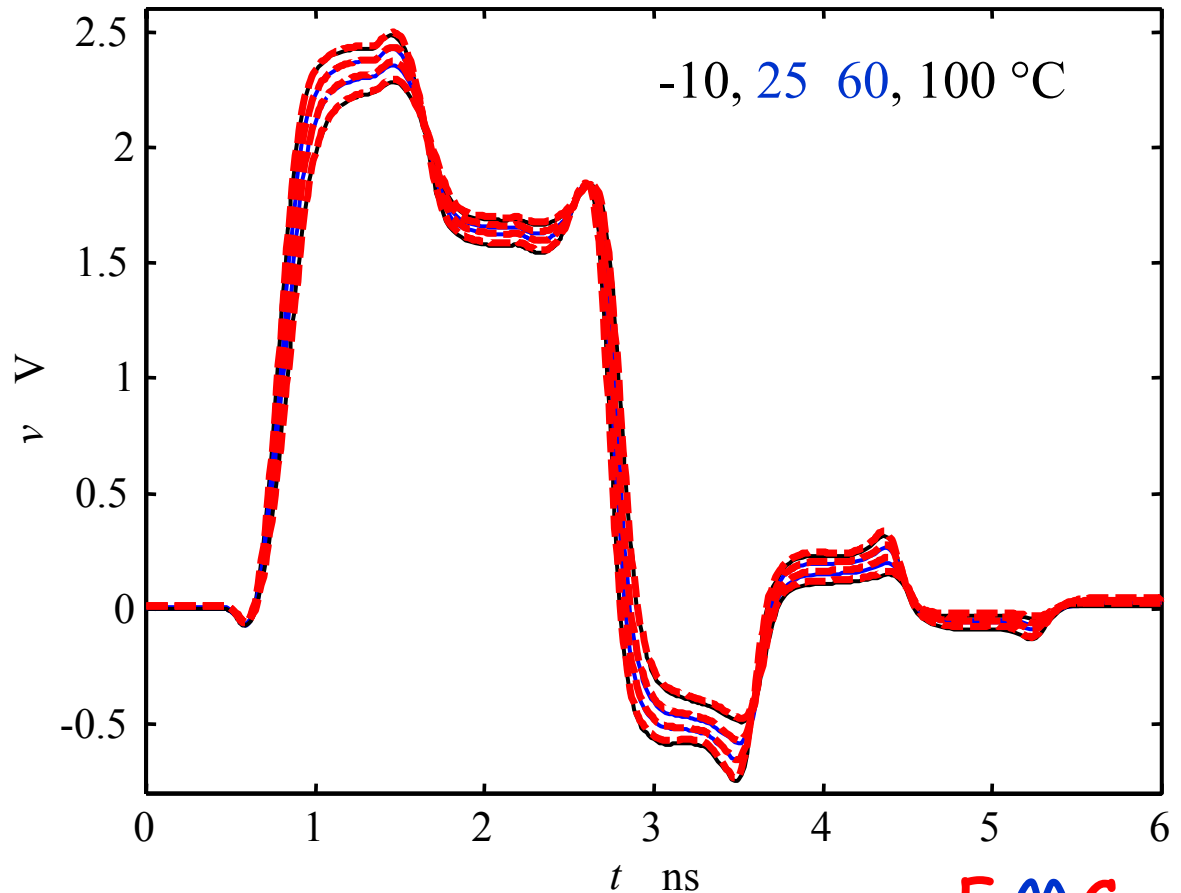
## Example #2: temperature effects

### • Test Case



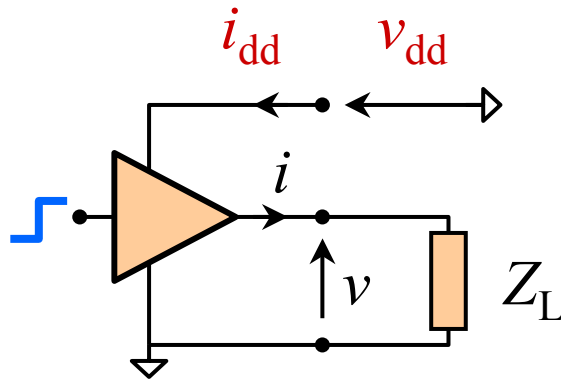
accuracy confirmed for realistic loads and a wide range of  $T$  values

$T_{\text{MIN}} = 10^\circ\text{C}$ ,  $T_{\text{TYP}} = 40^\circ\text{C}$ ,  $T_{\text{MAX}} = 80^\circ\text{C}$





# Integration of signal and power supply port behavior



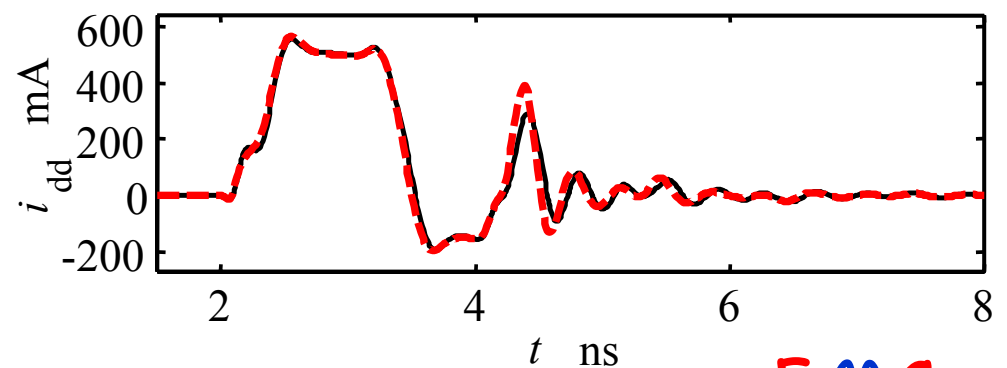
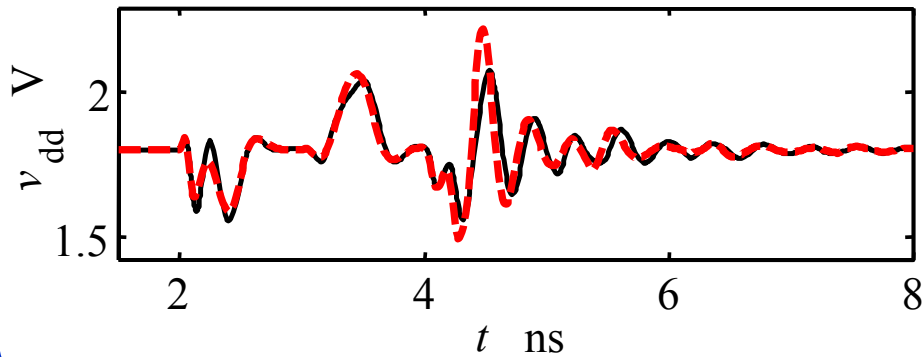
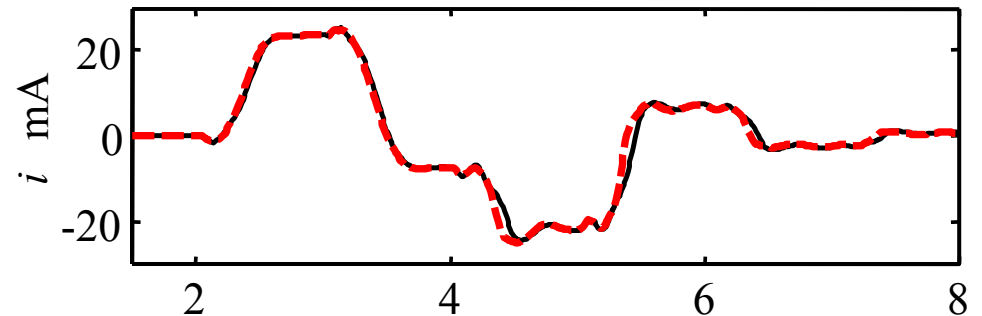
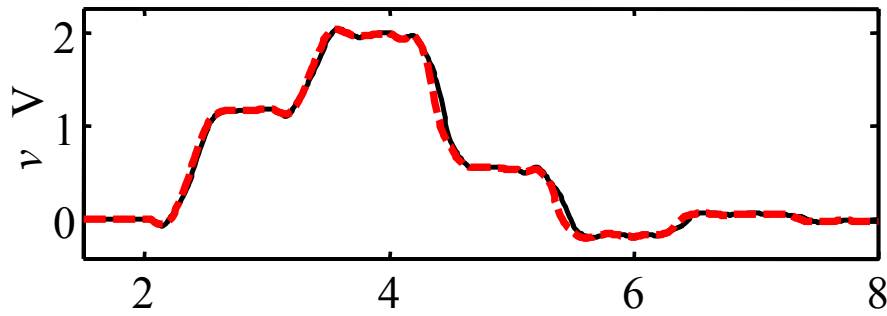
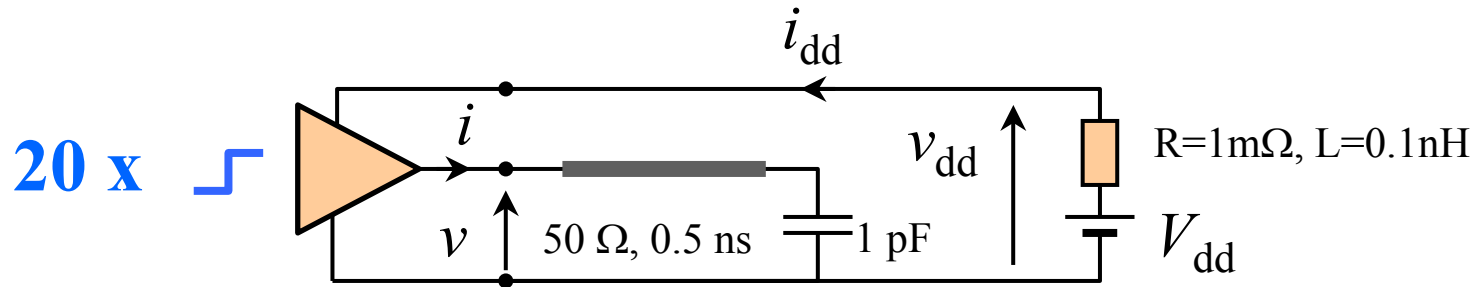
$$i = F(\Theta, v, v_{dd})$$

$$i_{dd} = F_{dd}(\Theta, v, v_{dd})$$

Macromodels obtained for  $v_{dd}$  values within the range  $V_{dd} \pm 15\%$



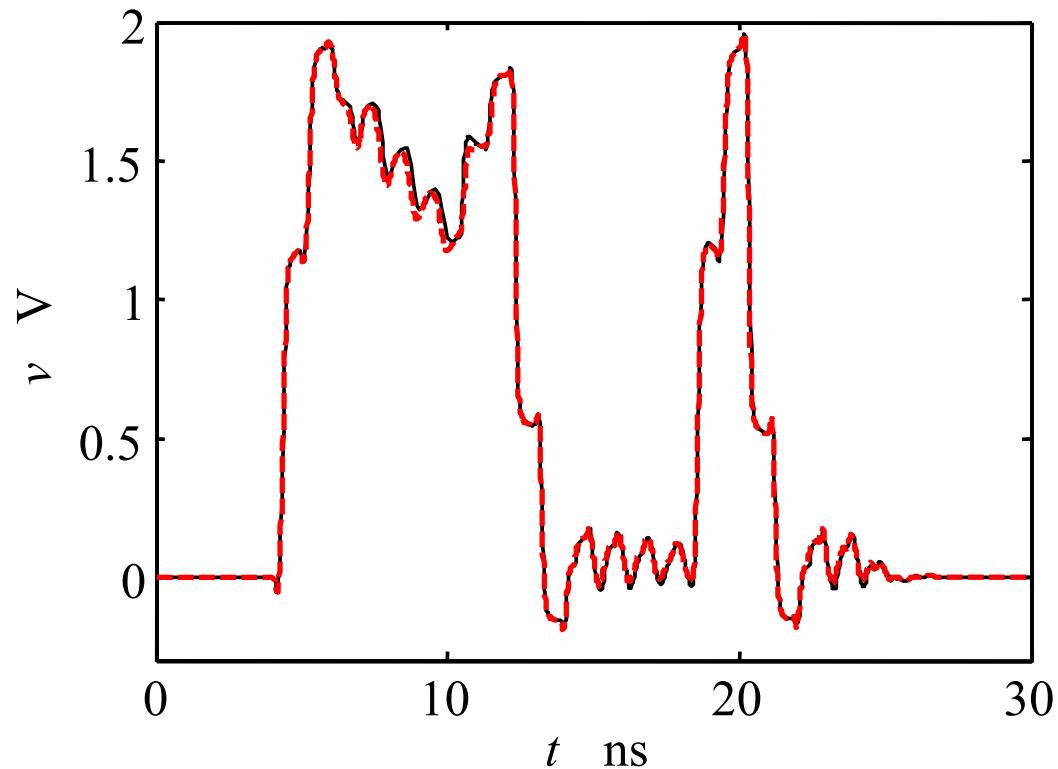
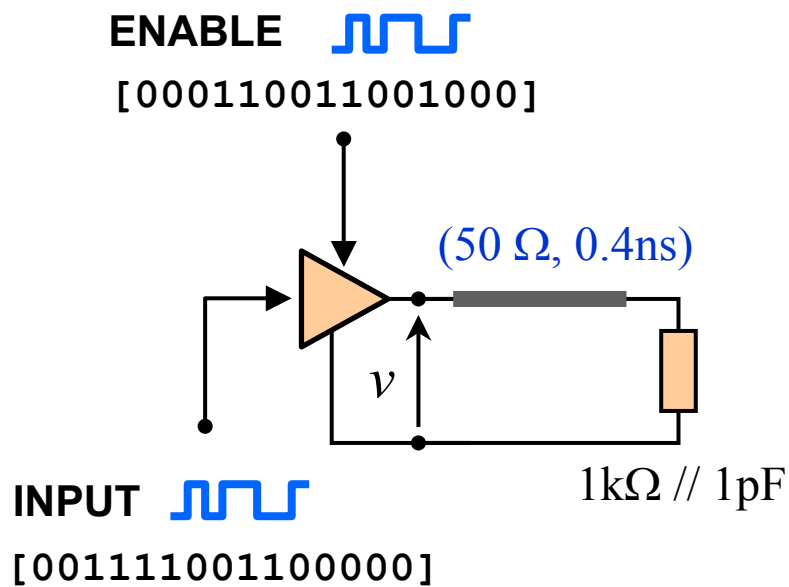
# Example #3: SSN analysis





## Example #4: tristate driver

- Test Case





# Conclusions

## ***Mπlog* approach**

- **Macromodels for I/O Buffers and Power Supply Ports of Digital ICs**
- **Advantages**
  - **PROTECTION OF IP**
  - **HIGH ACCURACY** (timing errors ~10 ps @ 400 MHz)
  - **LOW COMPLEXITY** (a few Gaussian functions)
  - **HIGH EFFICIENCY** (20÷100 time **faster** than transistor-level models)

**IBIS Compatibility via Multi-lingual description**