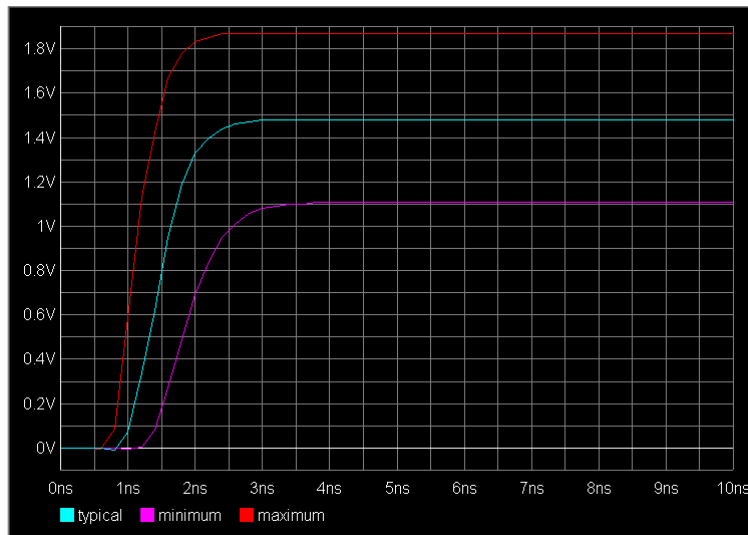


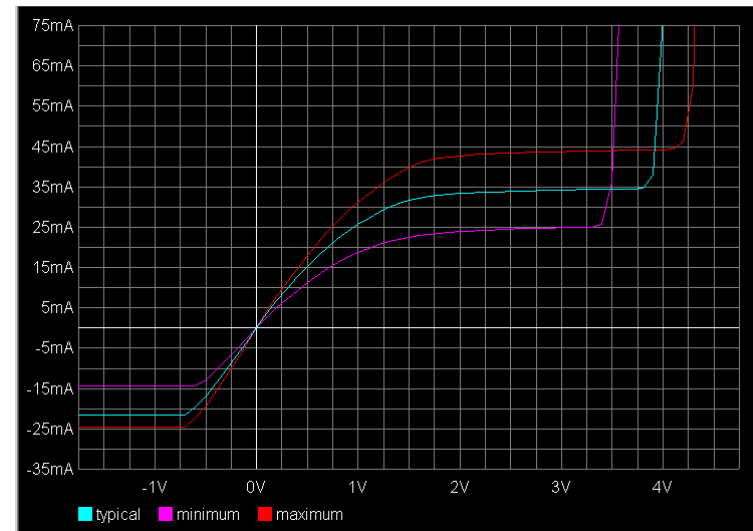
Things You Can Learn From V/I Curves

**IBIS Summit / DAC 2005
Todd Westerhoff
Cisco Systems, Inc.**

Components of a [Model] Declaration



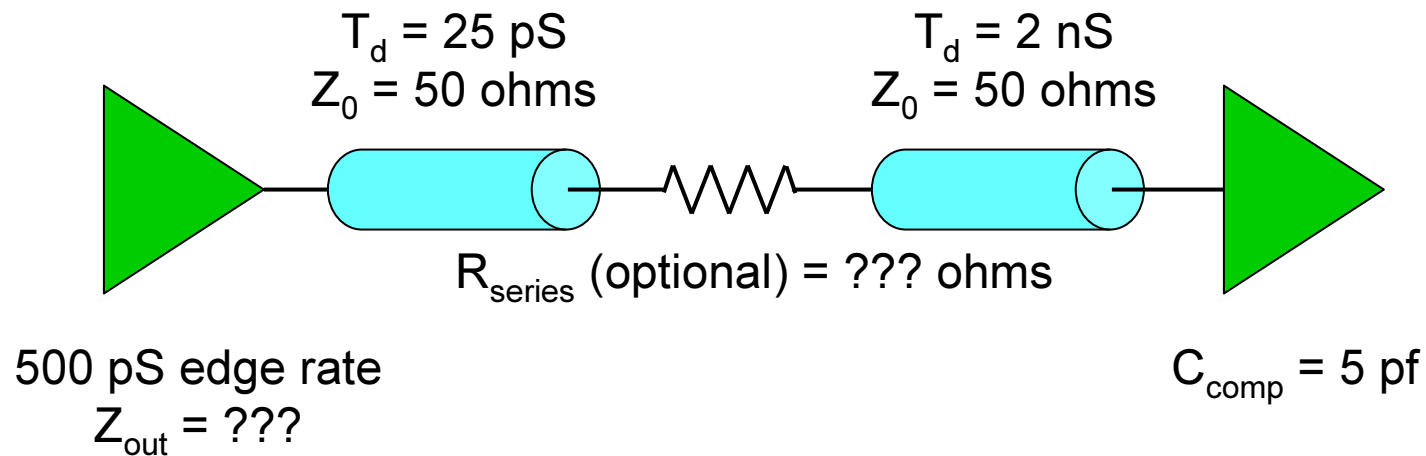
V/T Curves



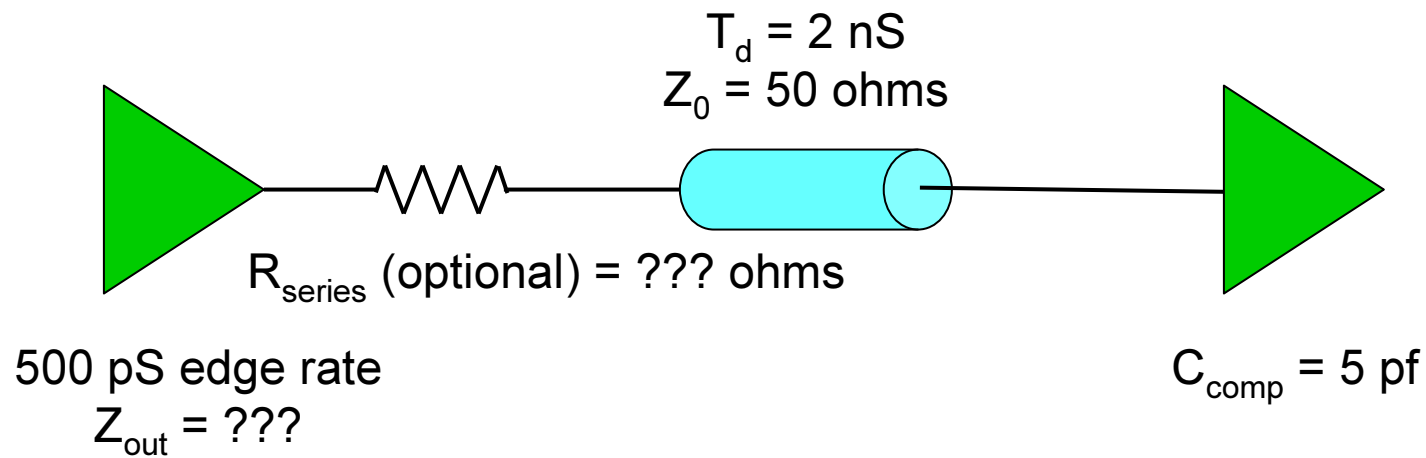
V/I Curves

- Pullup/Pulldown
- PWR/GND Clamps

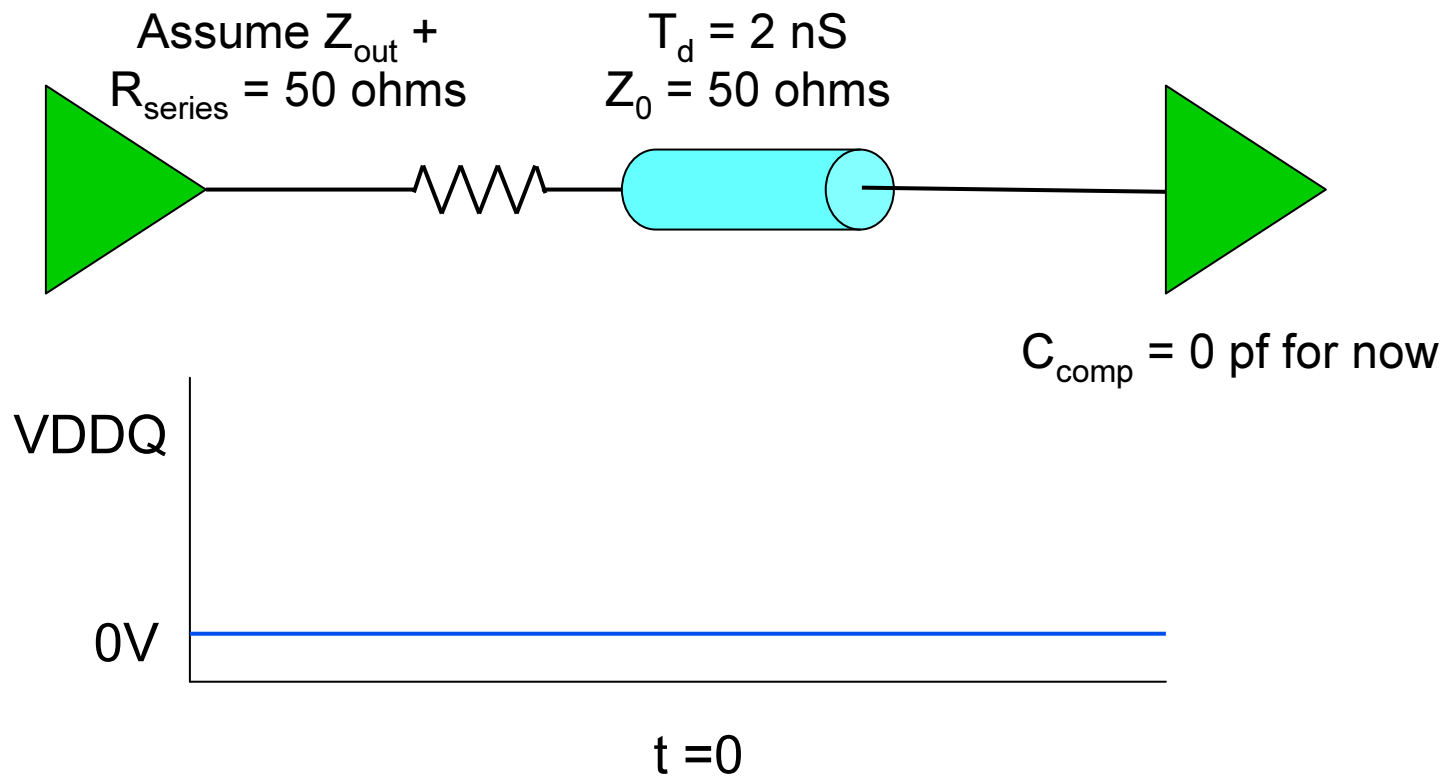
For Purposes of this Presentation ...



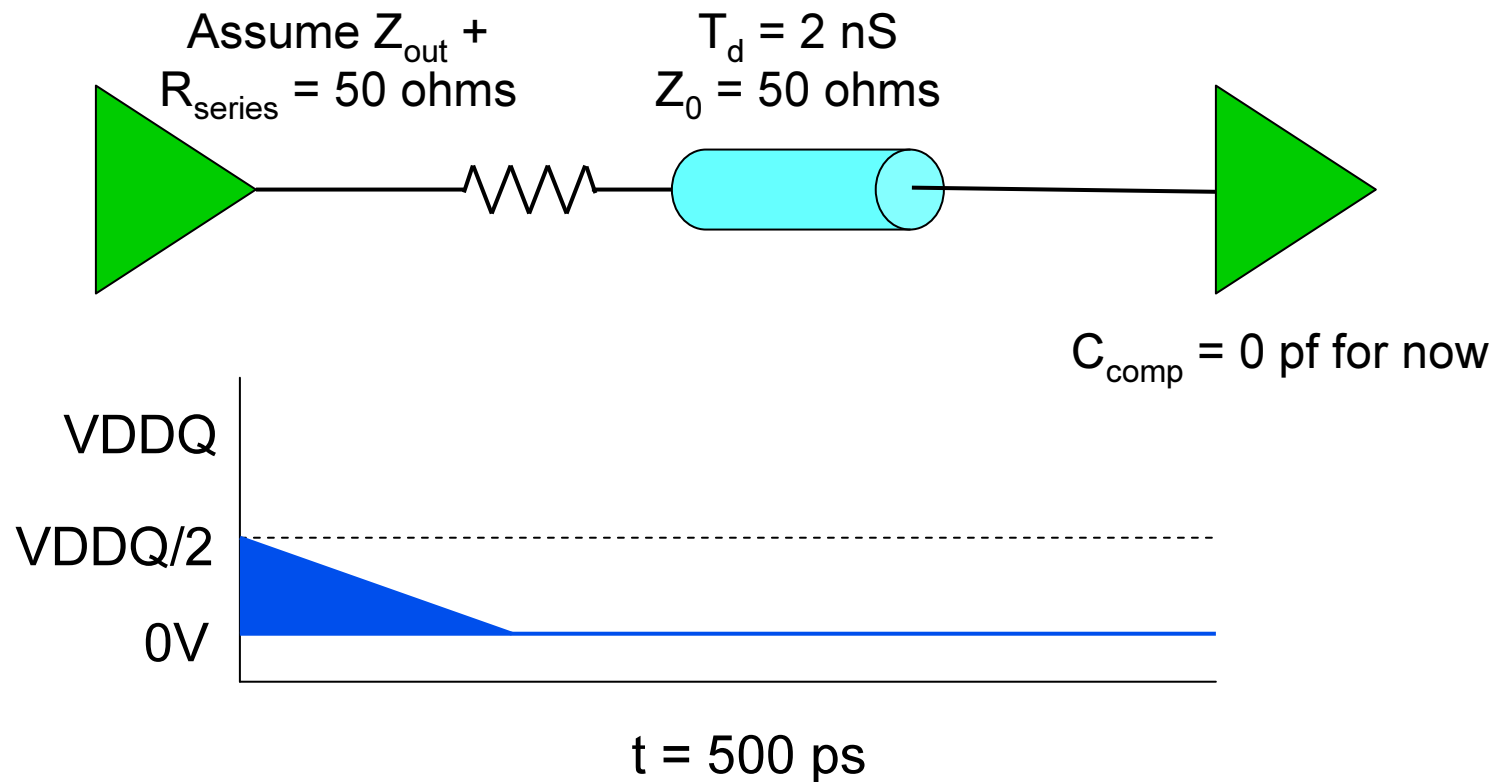
Electrically ...



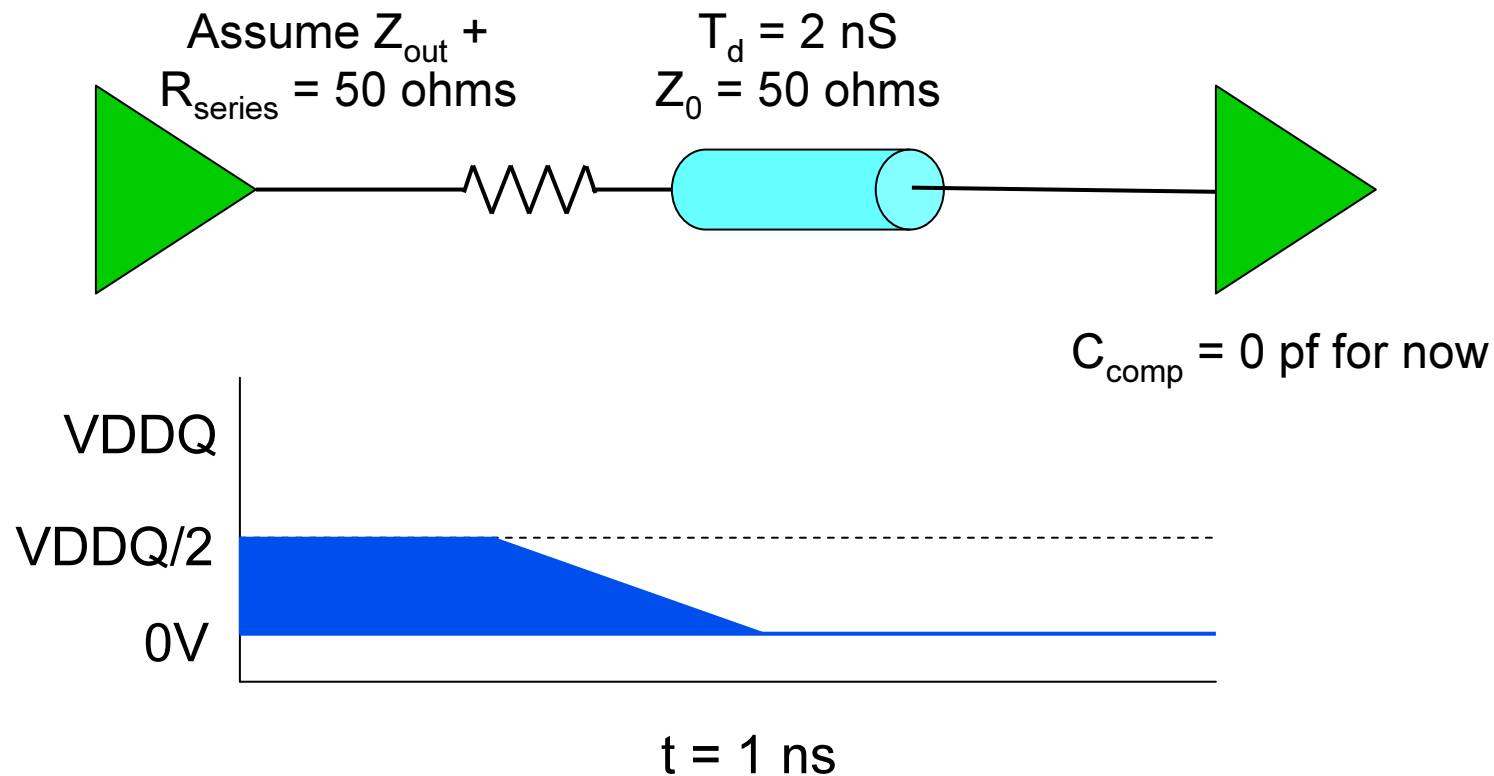
Rising Edge Behavior, $t=0$



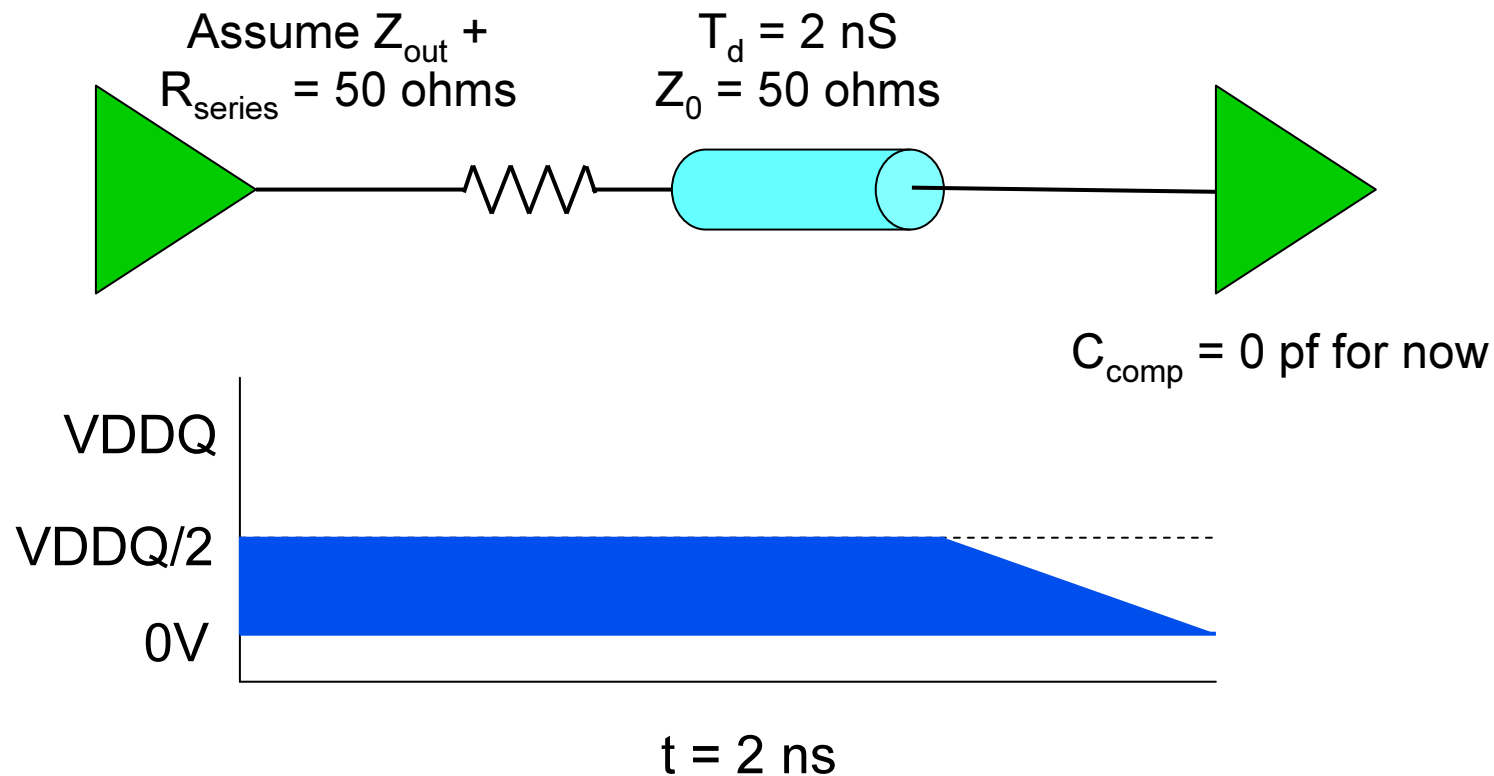
Rising Edge Behavior, $t=500\text{ps}$



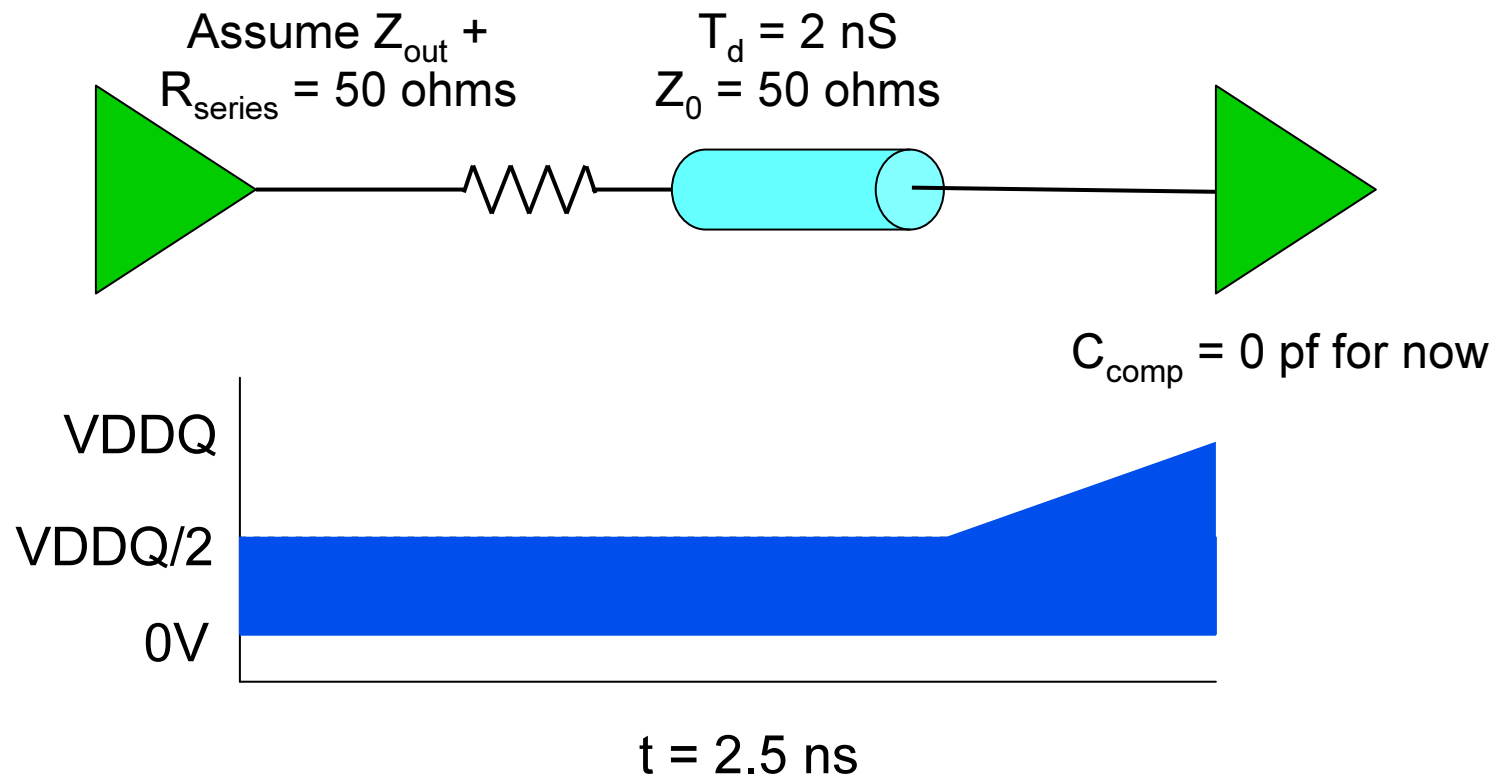
Rising Edge Behavior, $t=1\text{ns}$



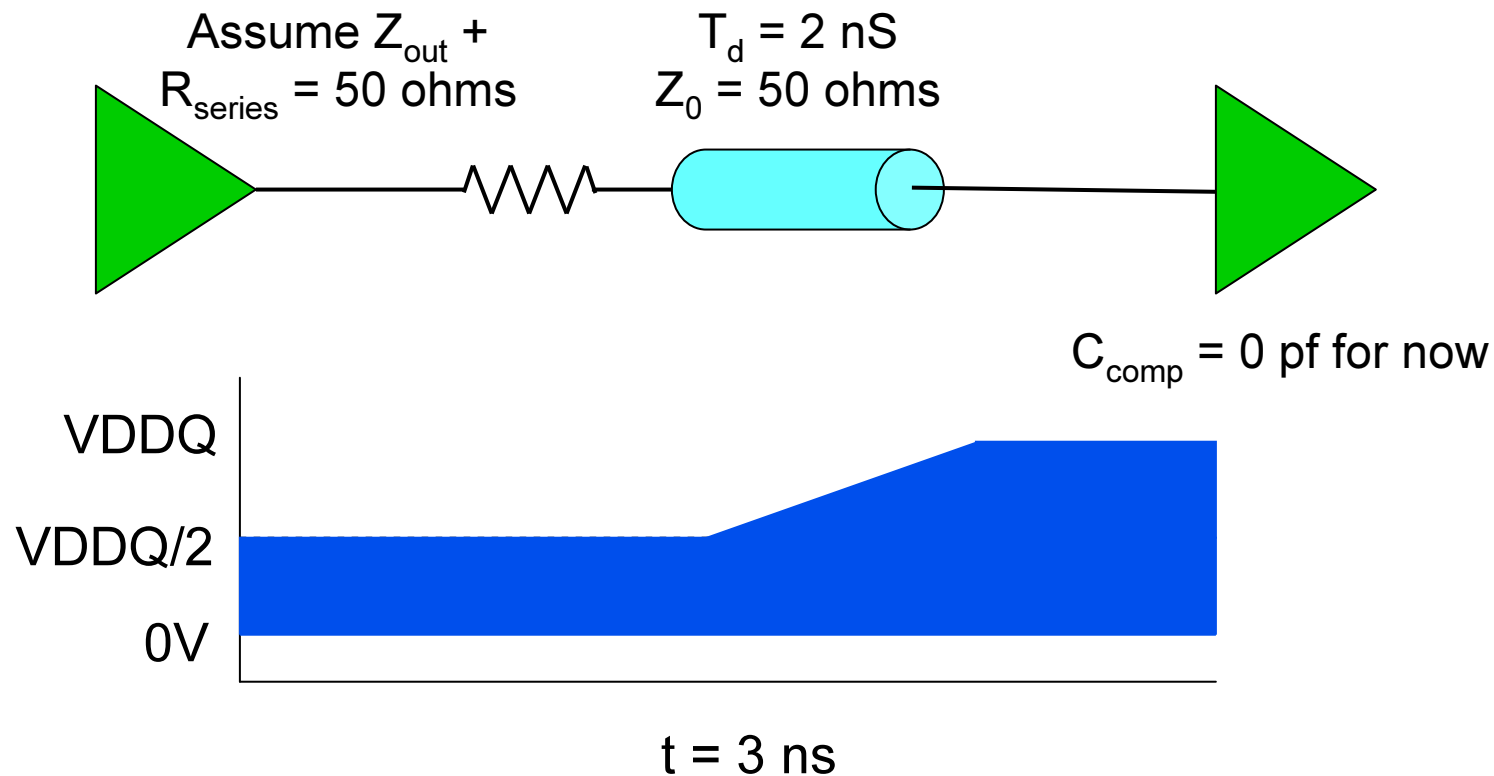
Rising Edge Behavior, $t=2\text{ns}$



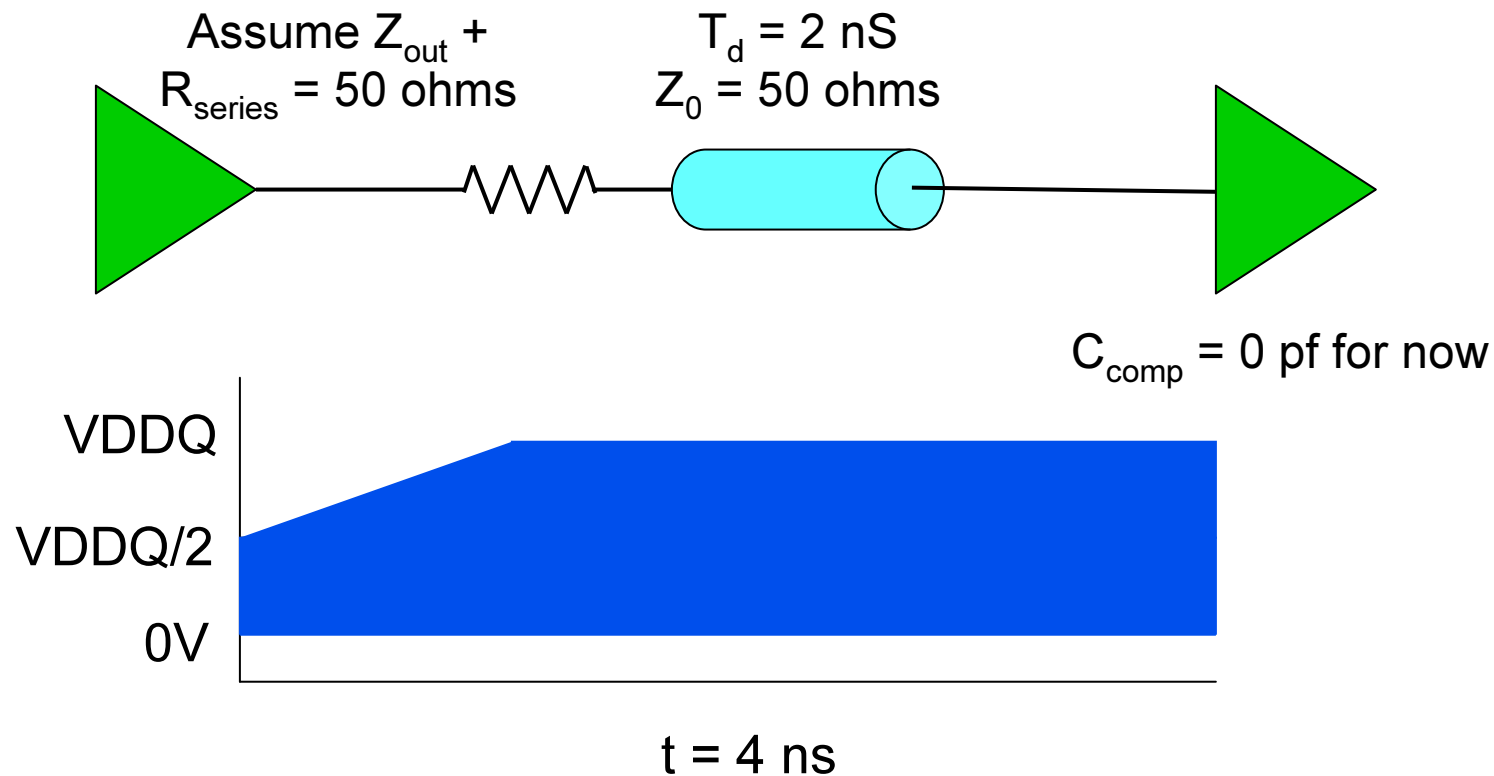
Rising Edge Behavior, $t=2.5\text{ns}$



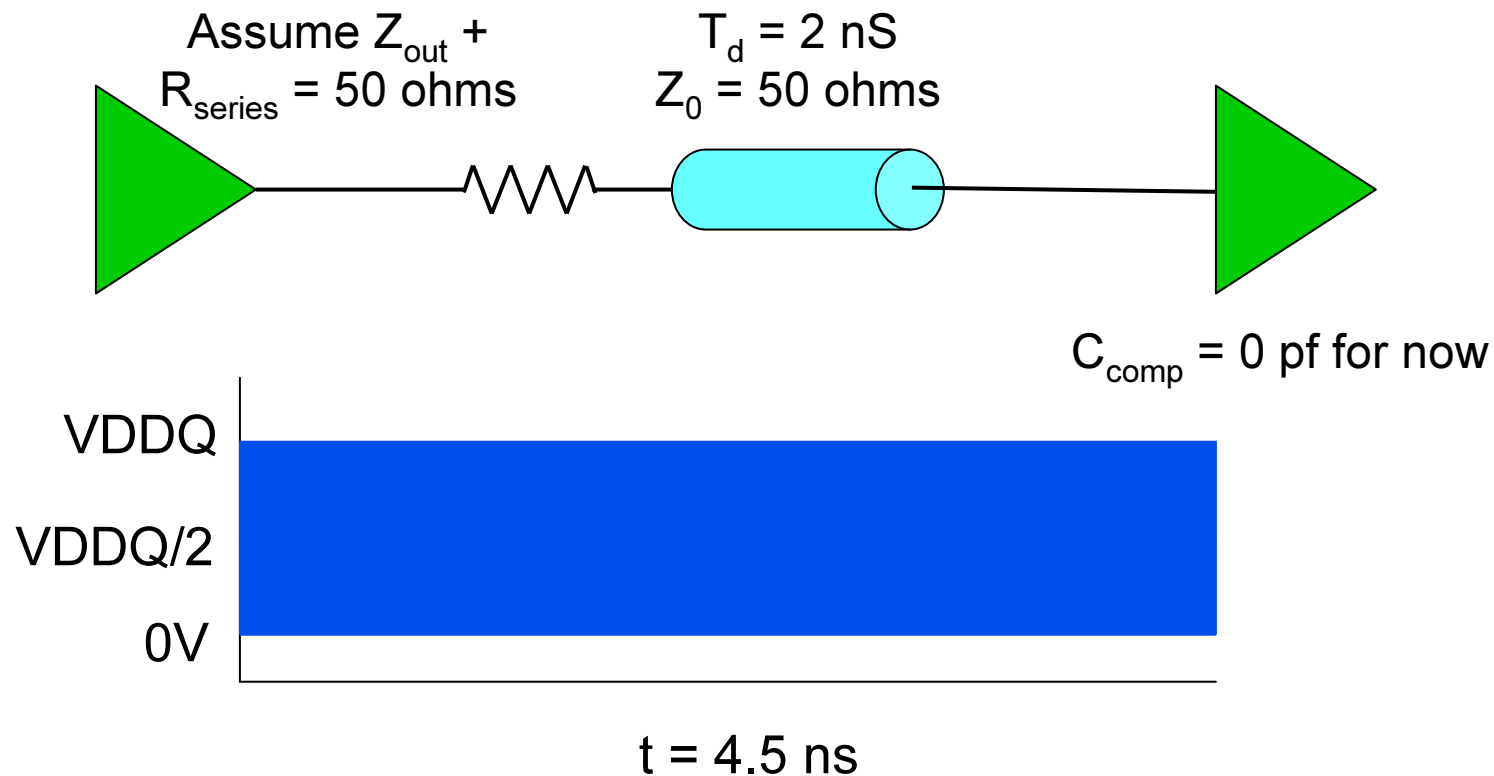
Rising Edge Behavior, $t=3\text{ns}$



Rising Edge Behavior, $t=4\text{ns}$



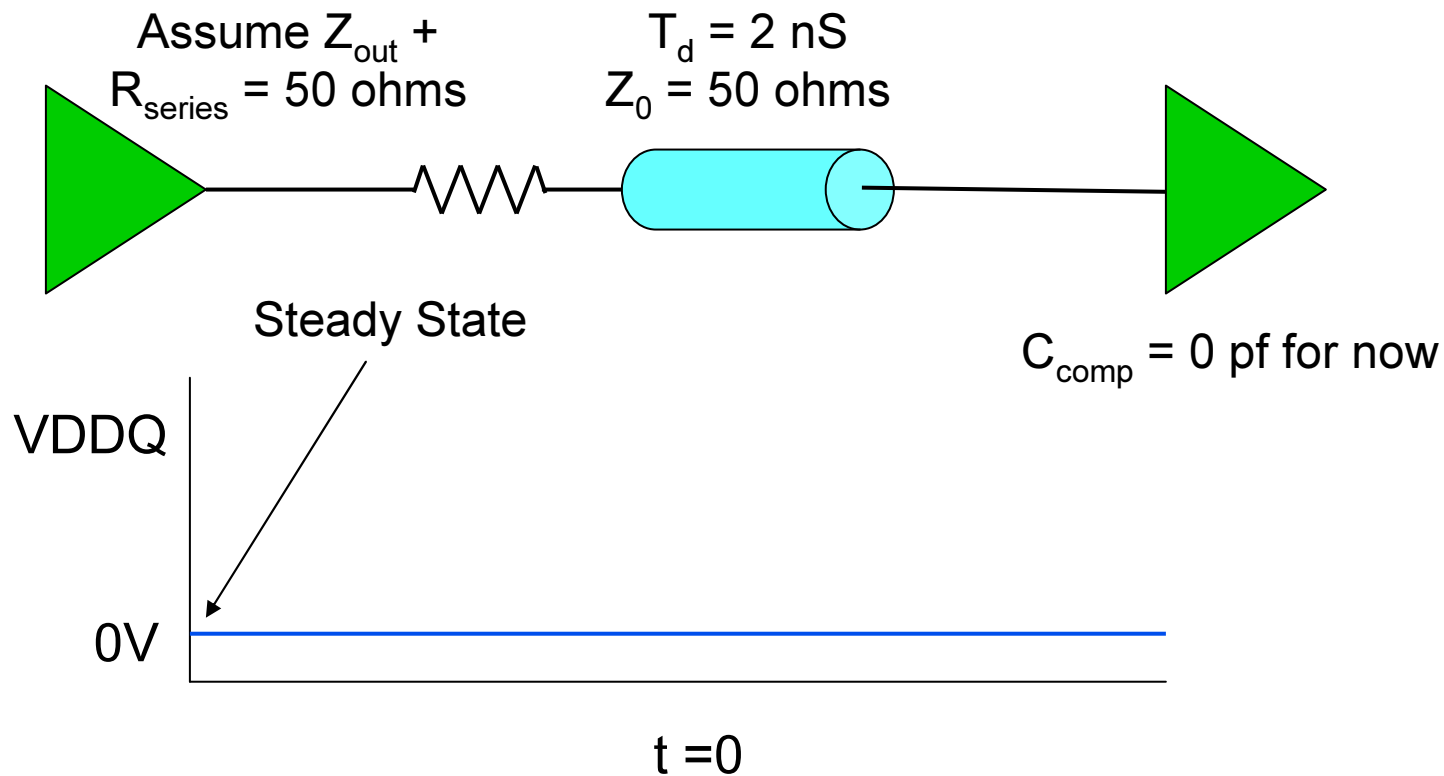
Rising Edge Behavior, $t=4.5\text{ns}$



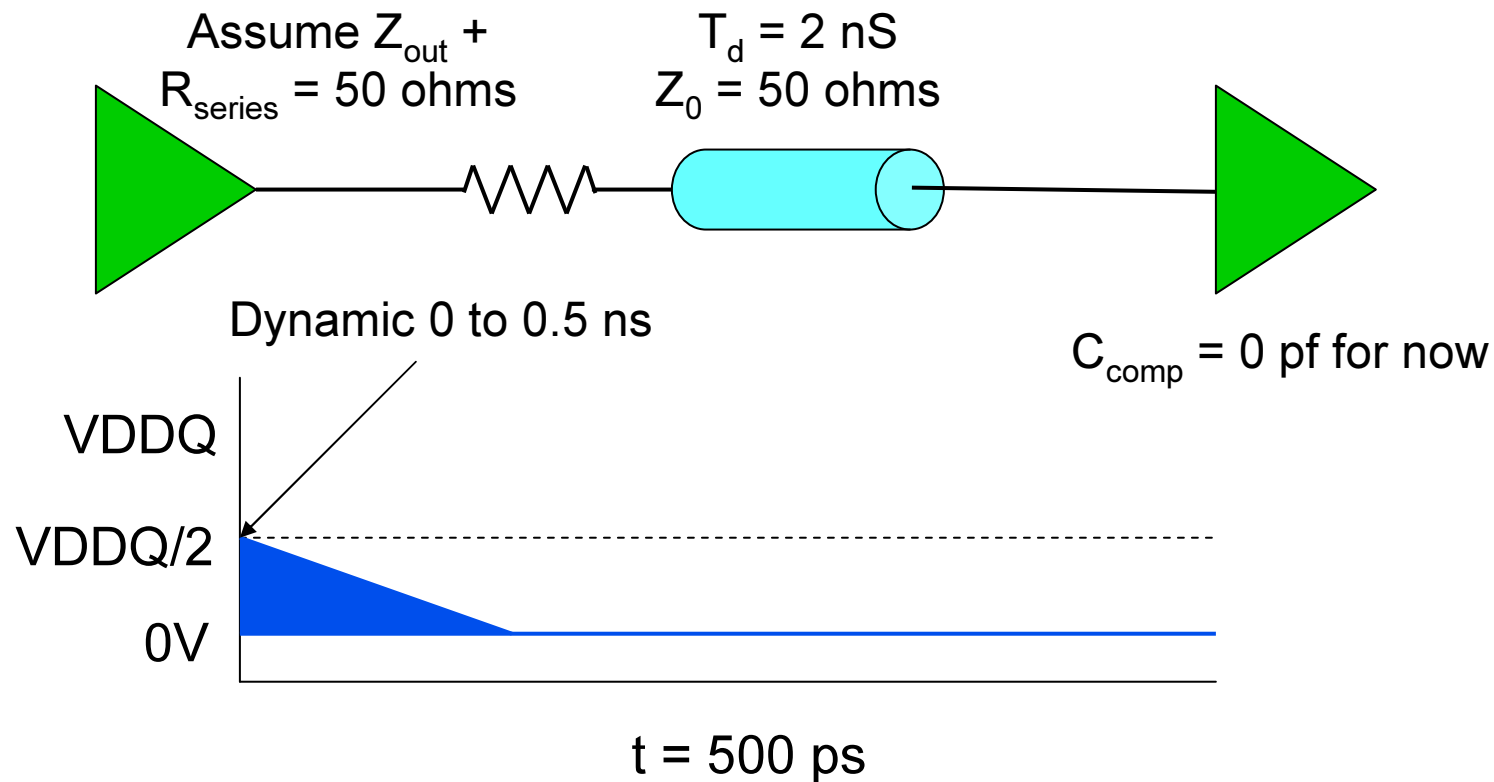
Observations

- **The buffer output changes voltage only when the edge is launched and the reflection is received**
 - Launch: 0 to 0.5 ns
 - Reflection: 4 to 4.5 ns
- **The buffer spends most of its time in the steady-state condition, where behavior is determined by the V/I curve**
 - Reflection behavior is also determined by the V/I curve

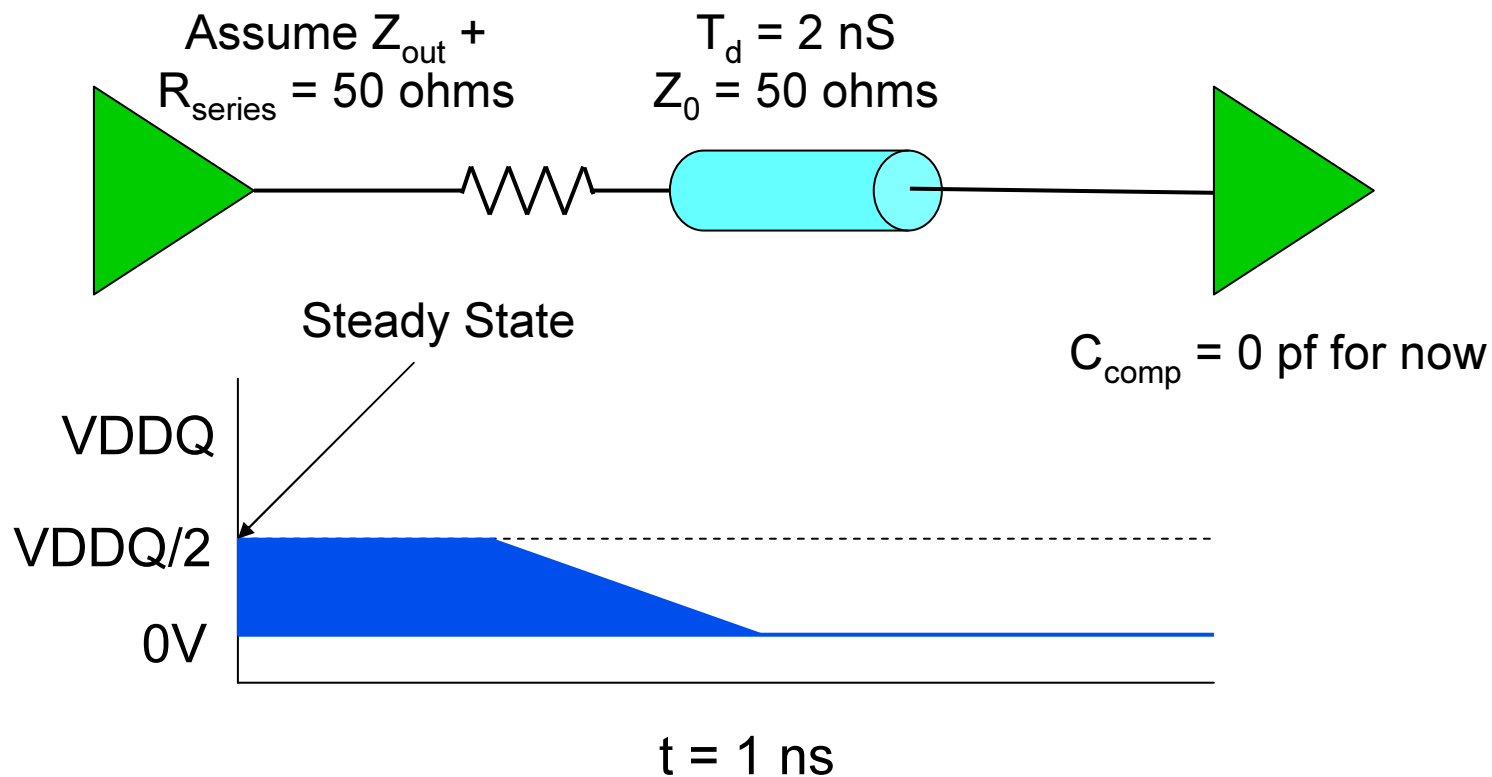
Dynamic vs. Steady State Behavior



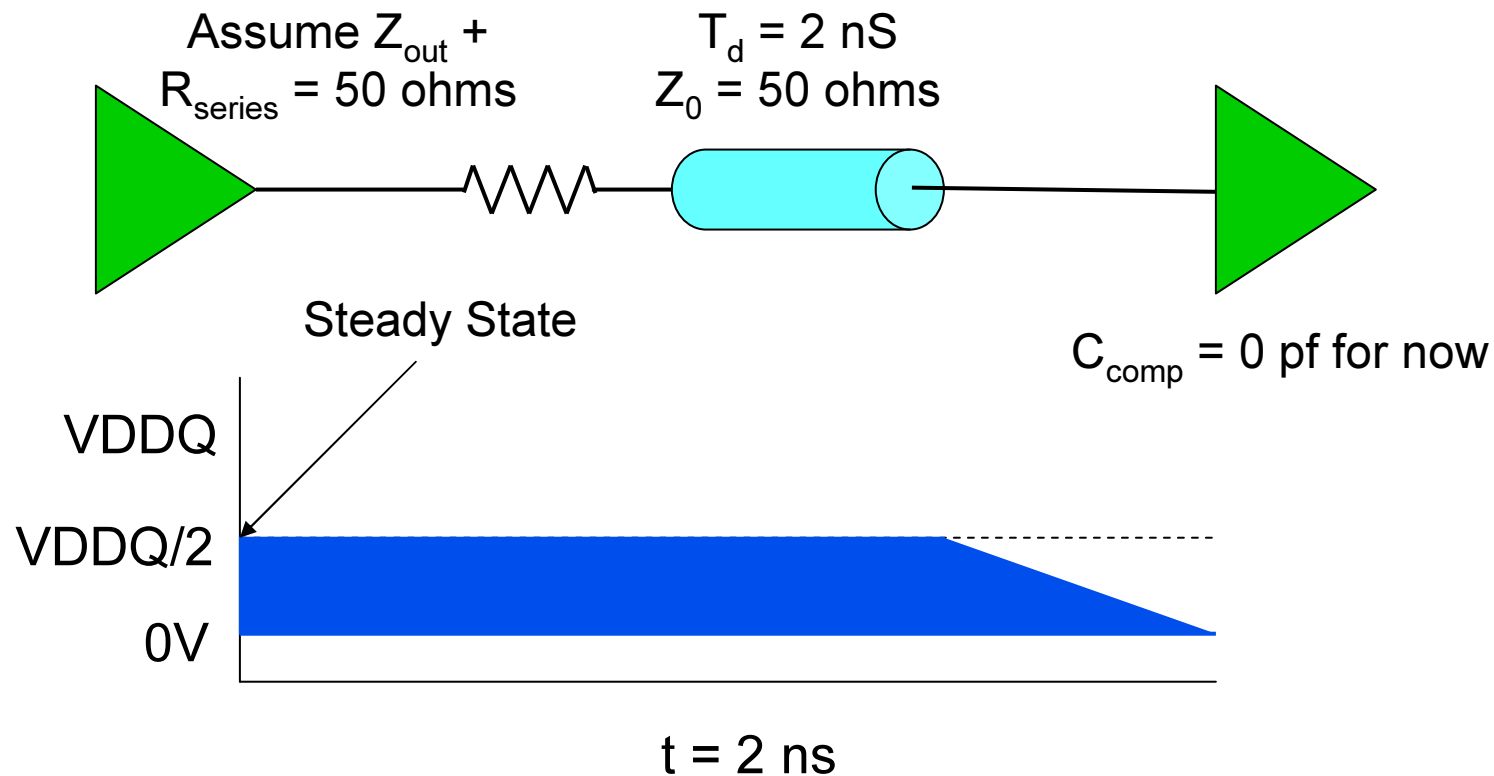
Dynamic vs. Steady State Behavior



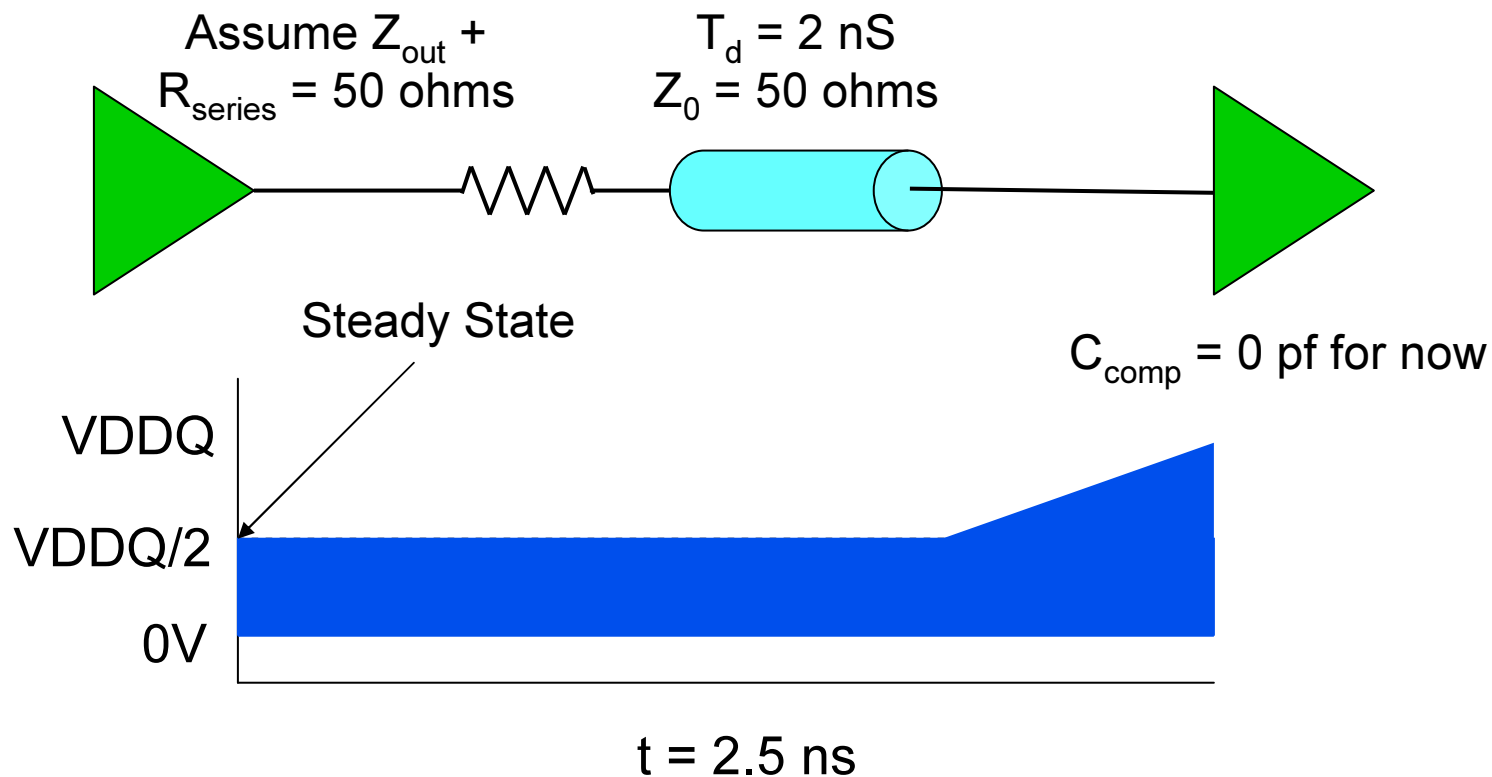
Dynamic vs. Steady State Behavior



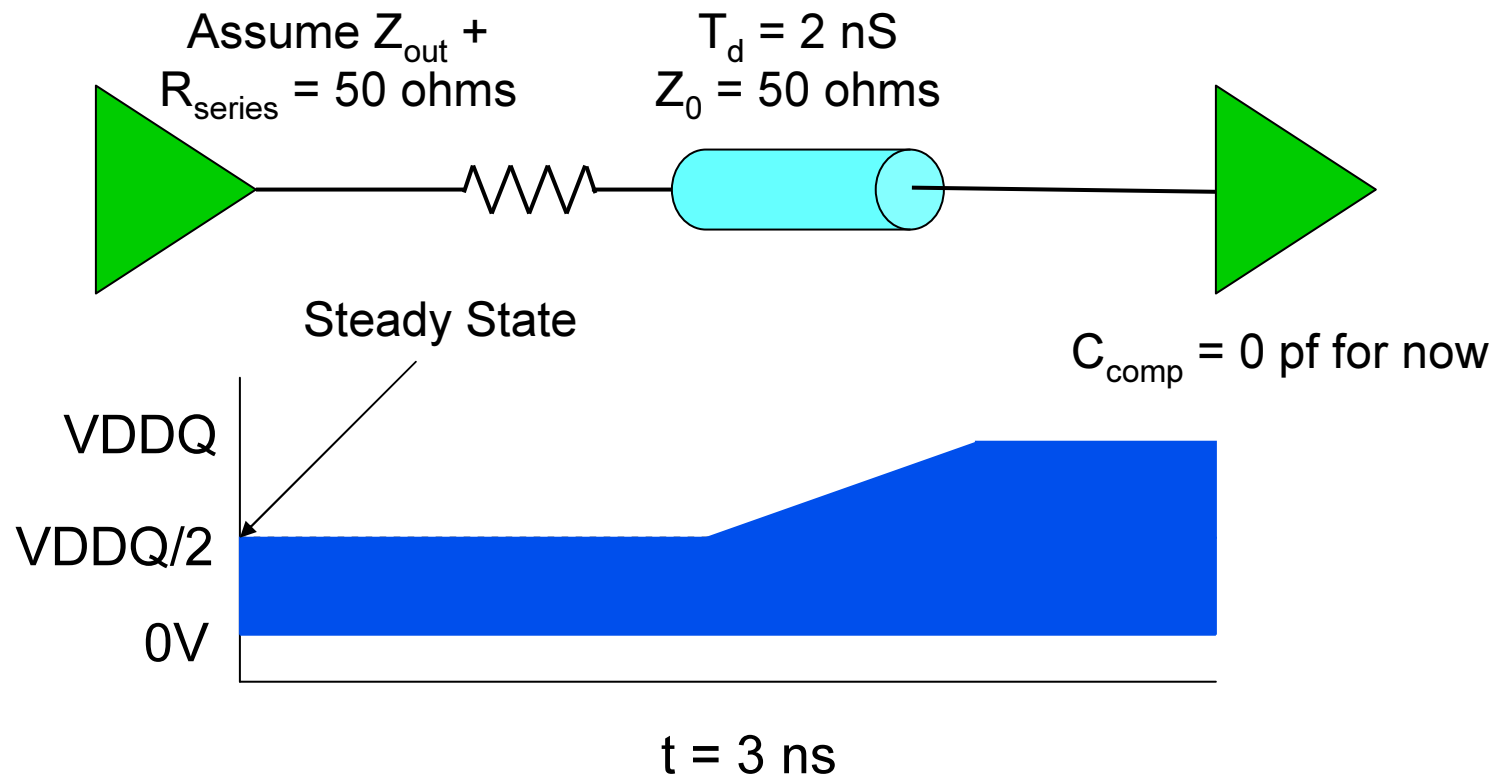
Dynamic vs. Steady State Behavior



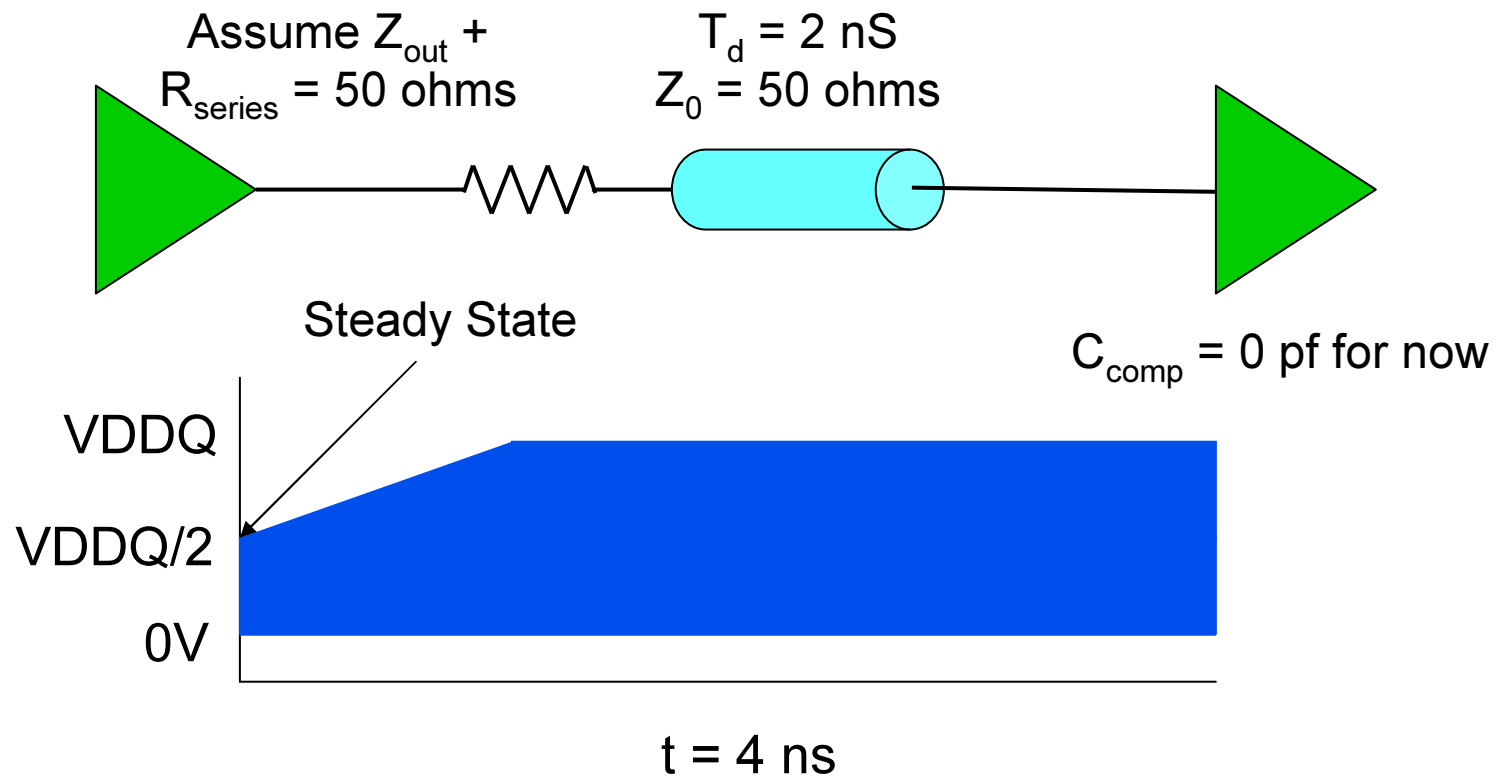
Dynamic vs. Steady State Behavior



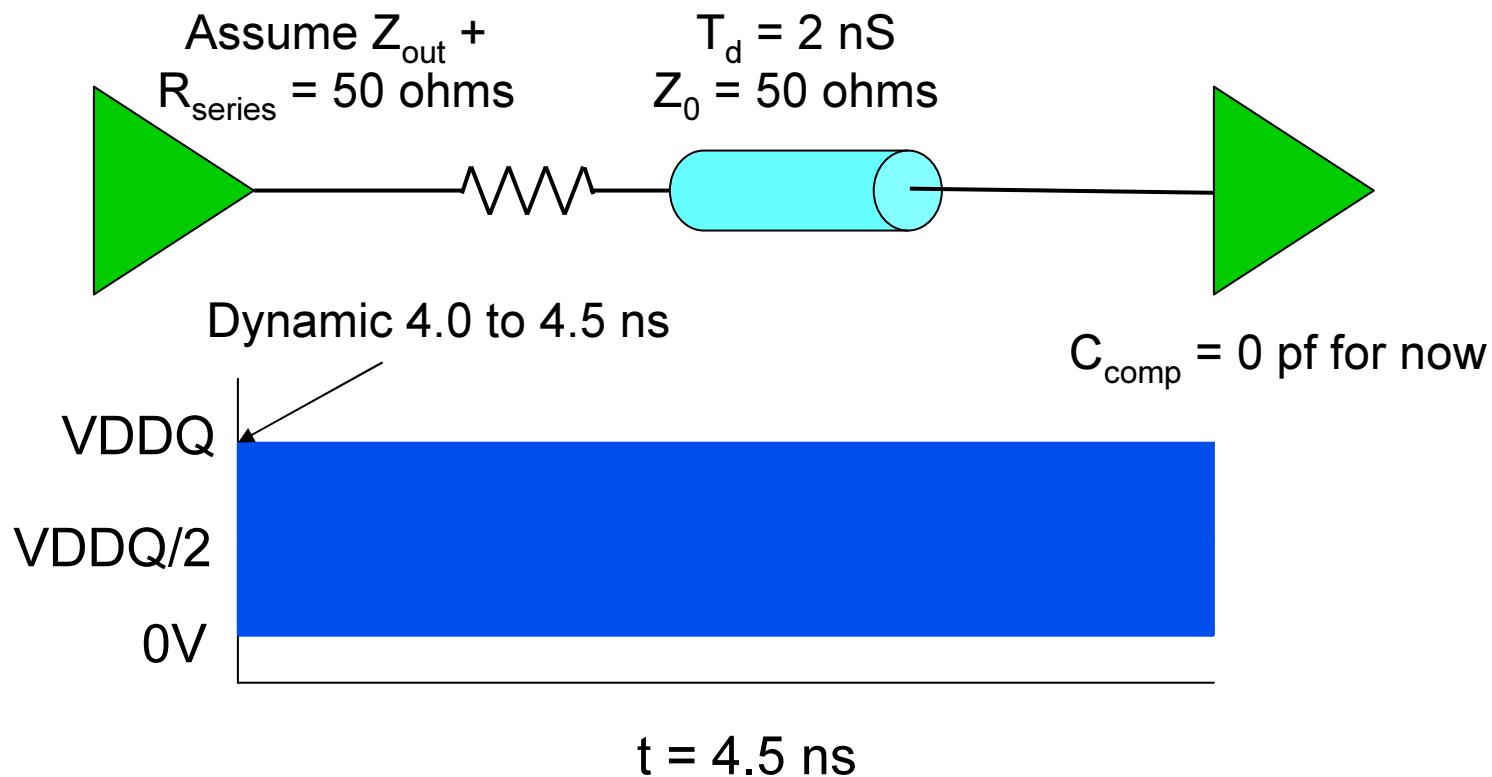
Dynamic vs. Steady State Behavior



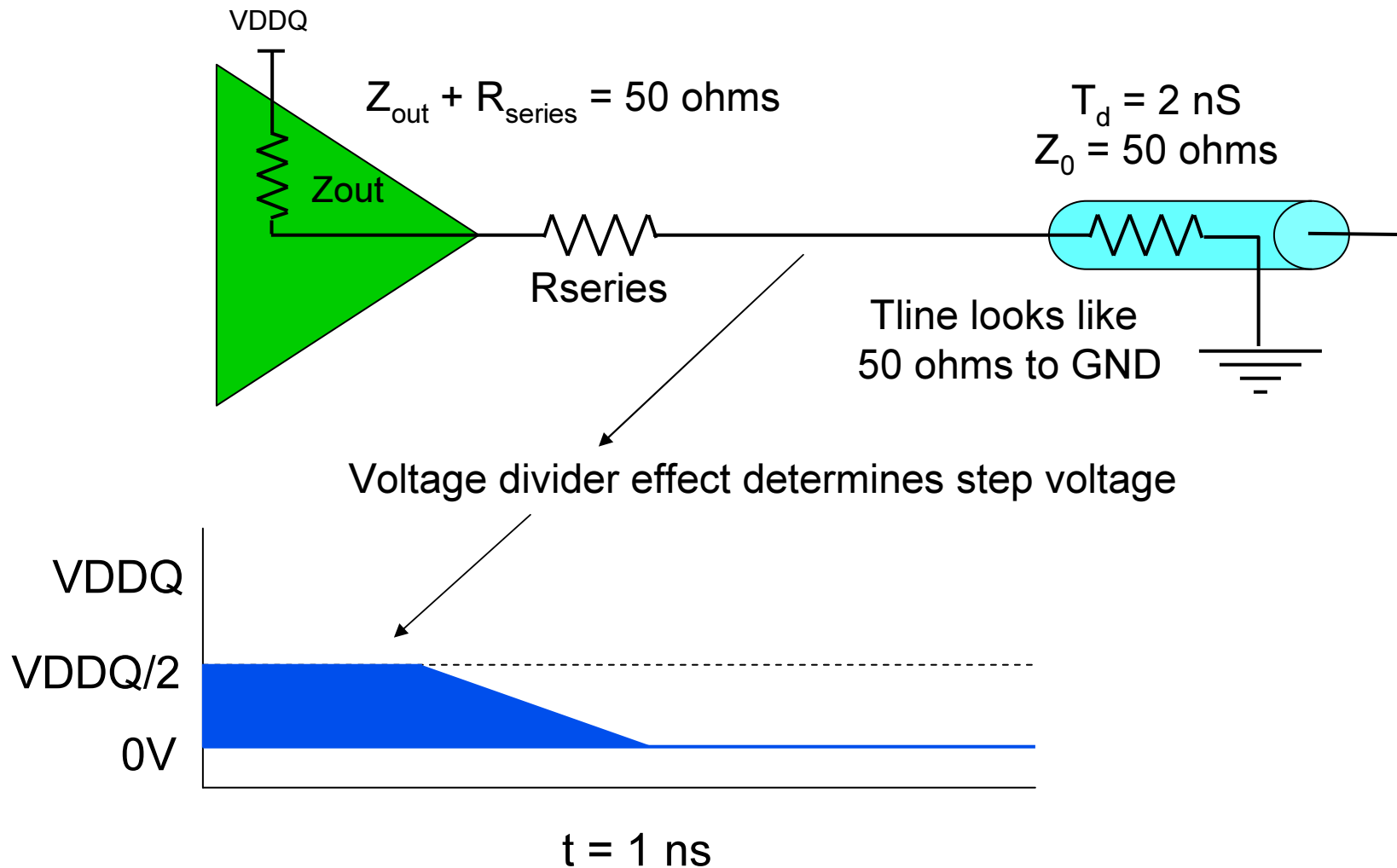
Dynamic vs. Steady State Behavior



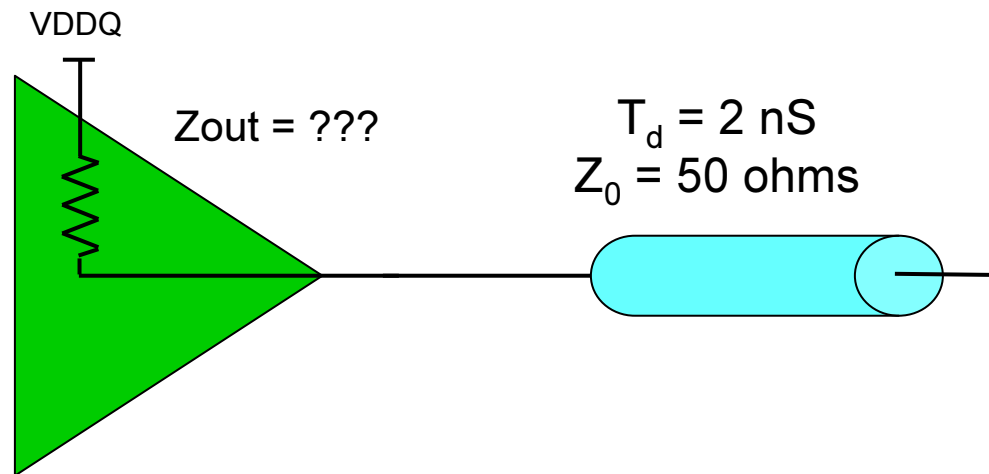
Dynamic vs. Steady State Behavior



... So What Determines Steady-State Values?



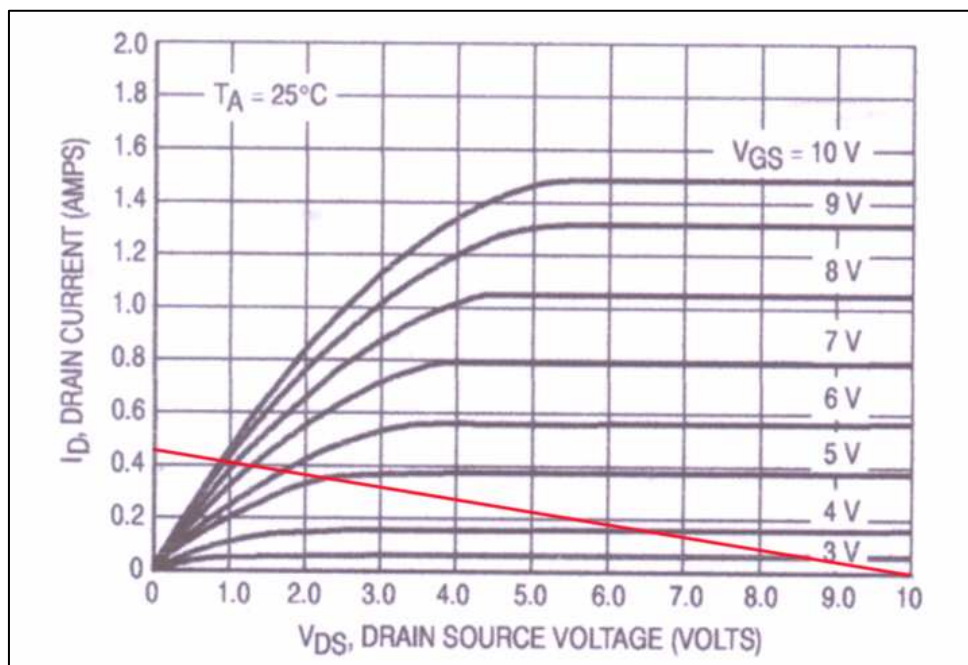
How to Determine Z_{out} ?



- If we know Z_{out} , we can compute step voltage
- Can select R_{series} such that $Z_{out} + R_{series} = Z_0$

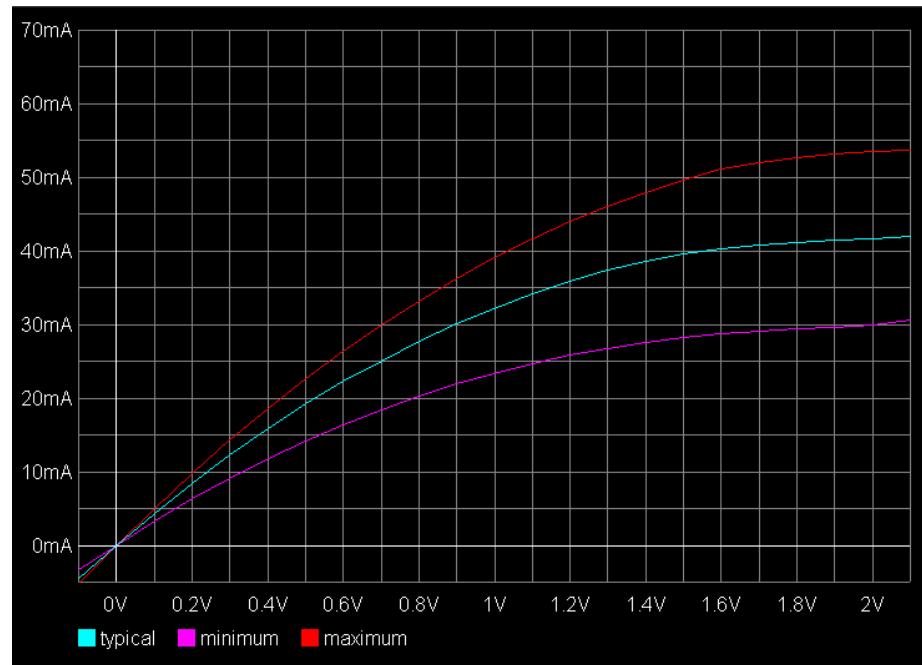
Remember Transistor Curves and Load Lines?

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- We used them to find DC bias points for amplifier circuits back in college
- They're equally valid for digital circuit analysis
 - Digital circuits simply operate with V_{GS} saturated

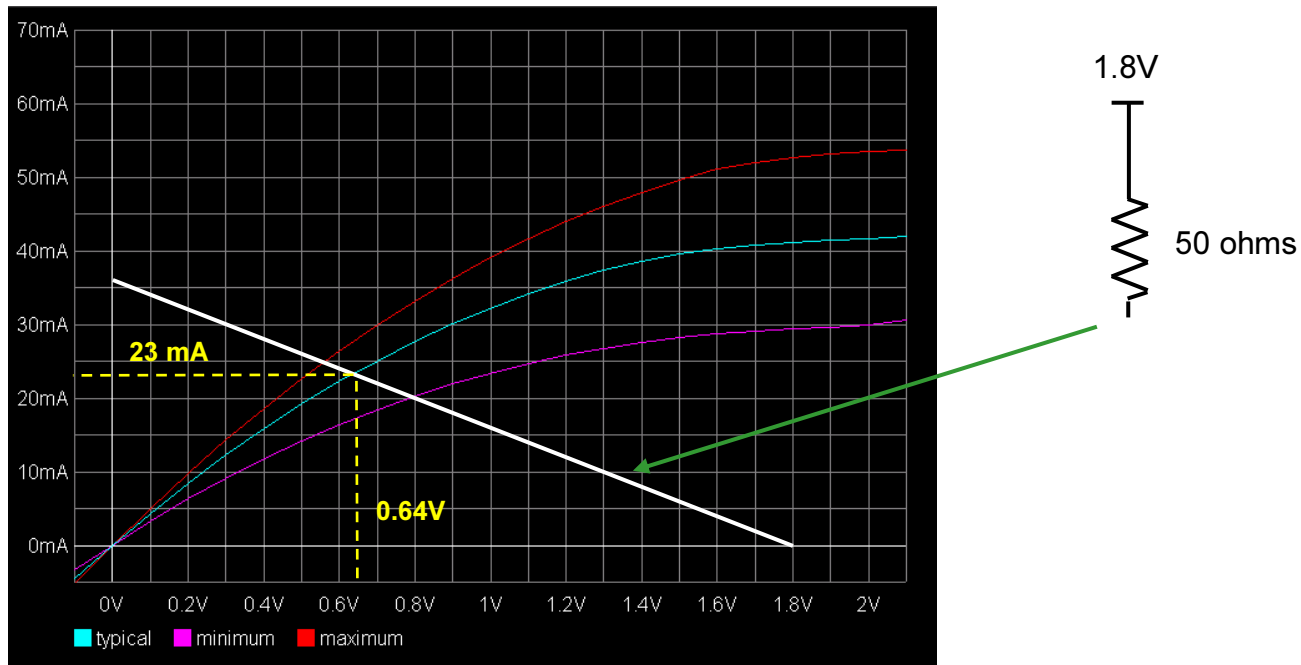
1.8V HSTL Class 1 Pulldown V/I Curve



- **Look like a transistor curve? That's because it is!**
 - Special case where $V_{GS} = V_{DDQ}$
- **Load line analysis will find the operating point**

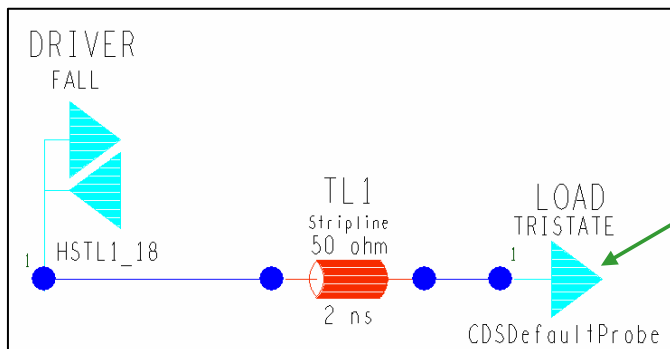
1.8V HSTL Class 1 Pulldown Load Line

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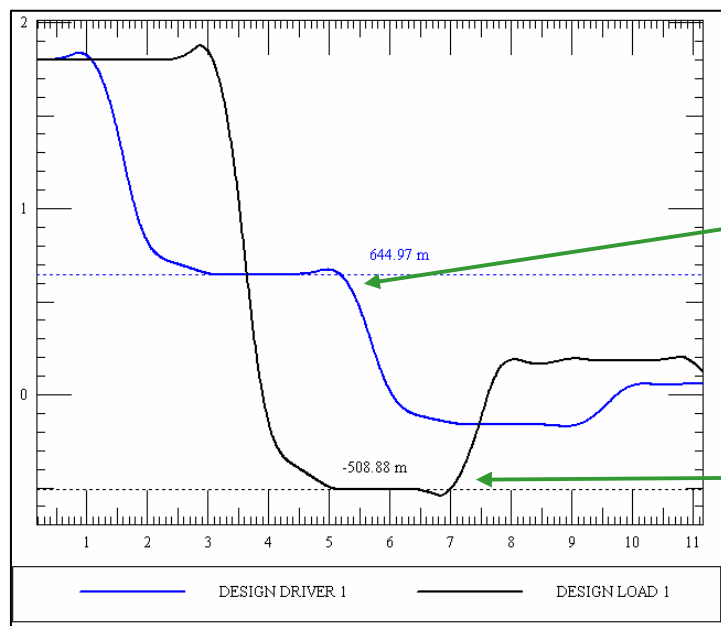


- Since this is a pull down, load line should be 50 ohms to VDDQ
- Step voltage for unterminated line is 0.64V
- This buffer will overdrive a 50 ohm line in the nominal case

Simulation Results



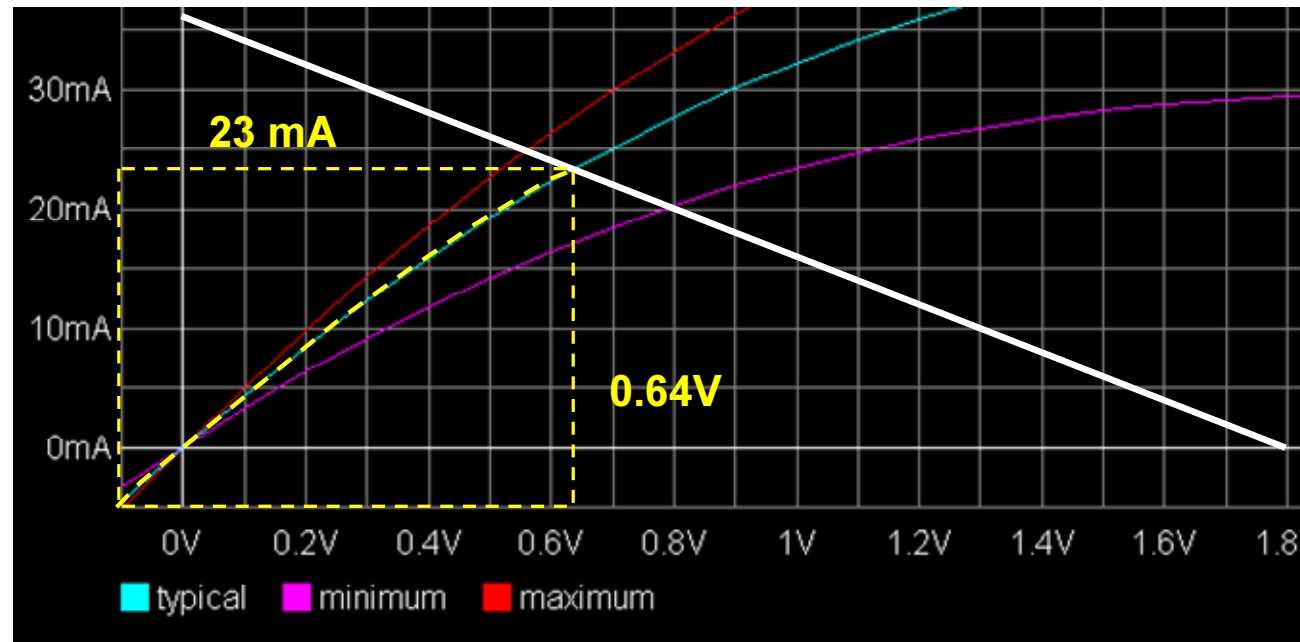
Dummy load has no effect; gives simulator a node to measure



Step voltage is 645 mV

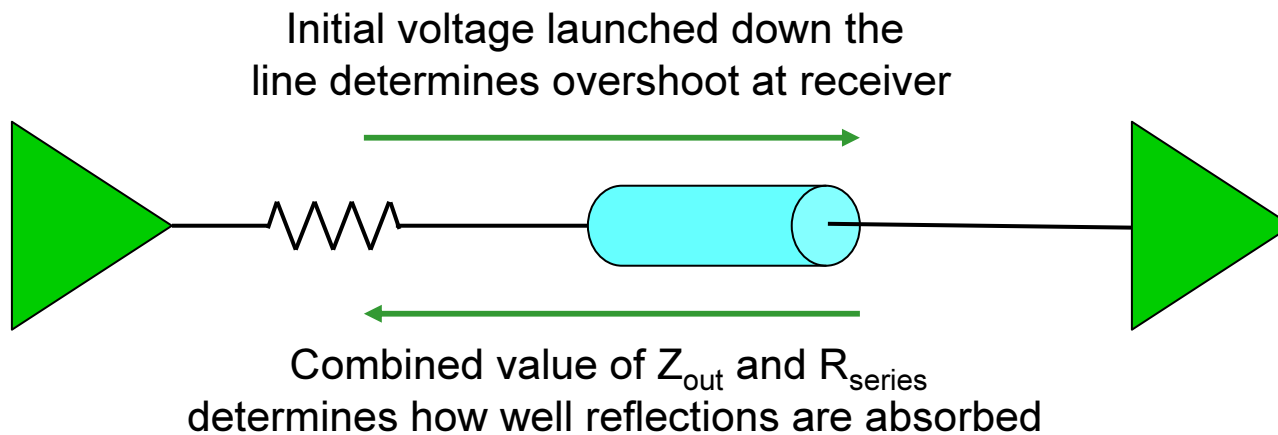
Overshoot is 509mV below GND

What Else Do We Know?



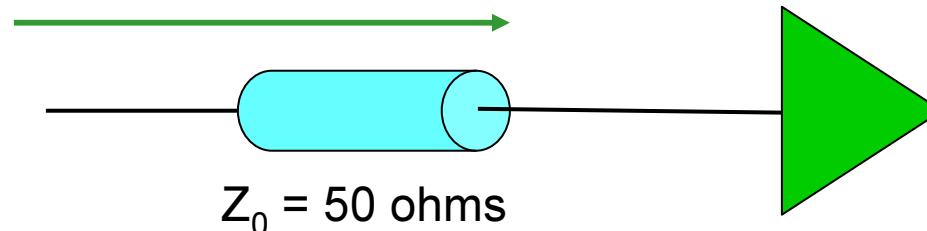
- **Pulldown will operate along the V/I curve from the origin to the load line intersection**
- **The slope of the V/I curve corresponds to Z_{out} , if the curve is linear, the device will behave as a resistor**

Serial Termination Basics



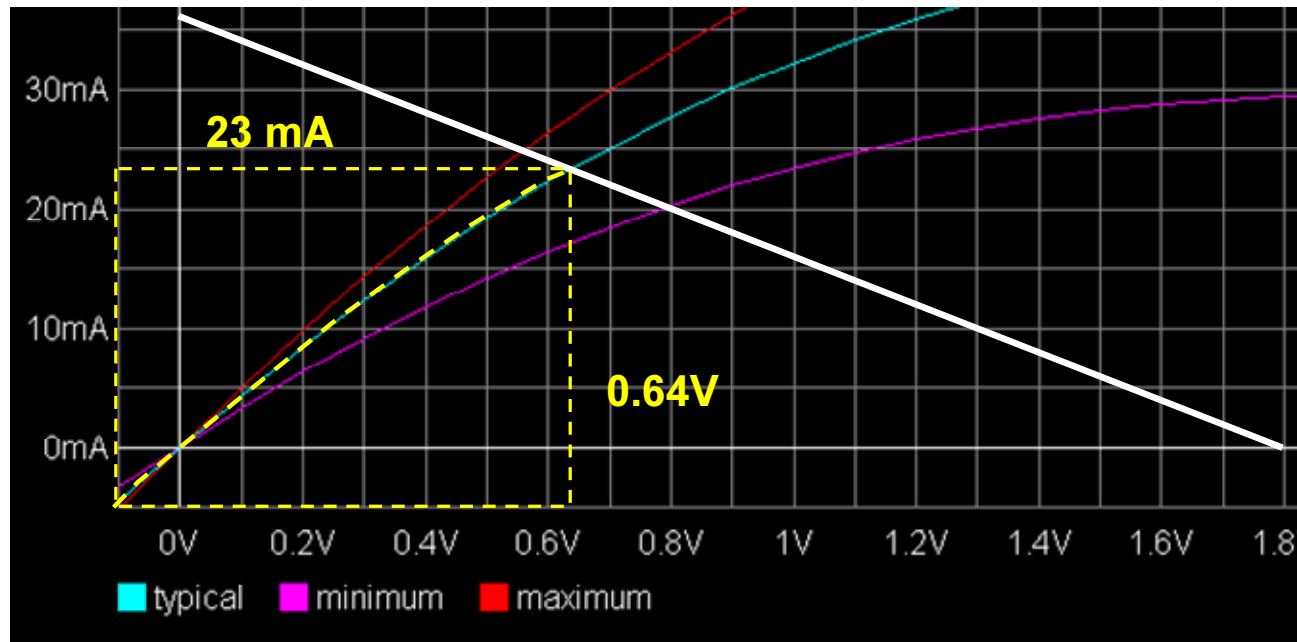
It's a Current Thing ...

What current gives us the ideal response at the receiver input?



- **Ideal step voltage is $V_{DDQ}/2$**
 - From Ohm's law: $E=IR$, $I=E/R$
 - $E = V_{DDQ}/2$, $R=50 \text{ ohms}$
 - $I = (V_{DDQ}/2)/50 = V_{DDQ}/100$
- **Our 1.8V receiver requires $1.8/100 = 18\text{mA}$ of line current for ideal reflection behavior**

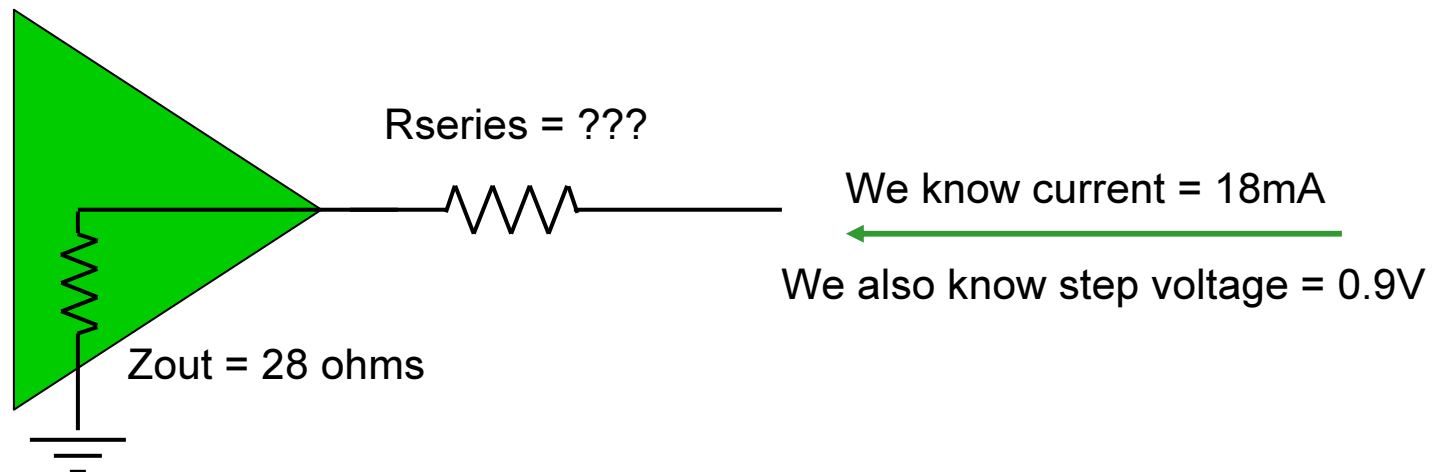
How Strong Is Our HSTL Output?



- **At 50 ohm operating point, $R=E/I$**
 - $E = 0.64V$, $I = 23 \text{ mA}$
- **Effective output impedance = 28 ohms**

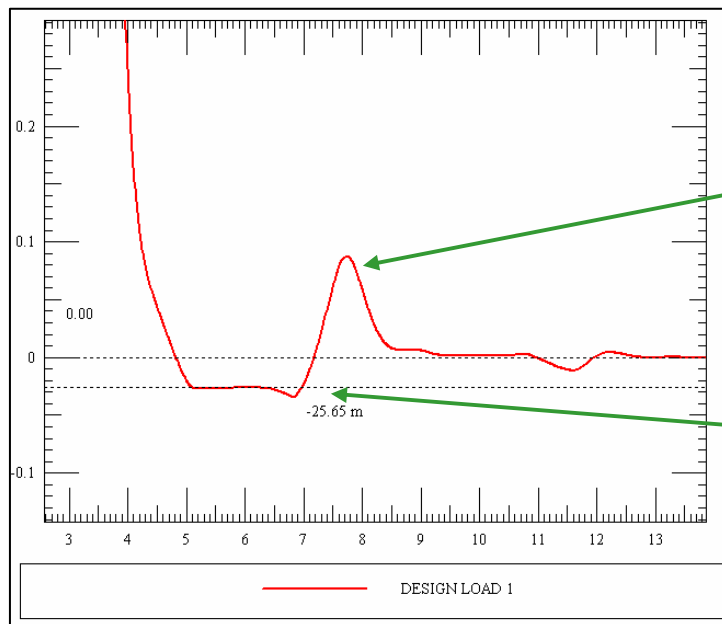
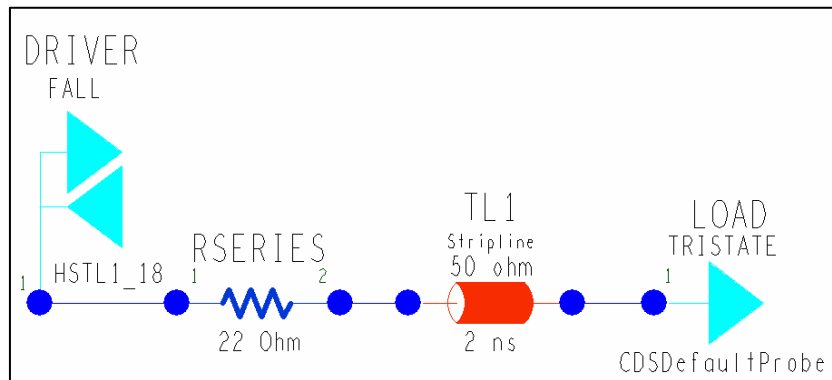
... So, What Value of R_{series} ?

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- **Effective Output Impedance, $R = E/I$**
 - $E = 0.9V$, $I = 18mA$, so $R = 50 \text{ ohms}$
- **$Z_{\text{out}} + R_{\text{series}} = 50$, $R_{\text{series}} = 22 \text{ ohms}$**

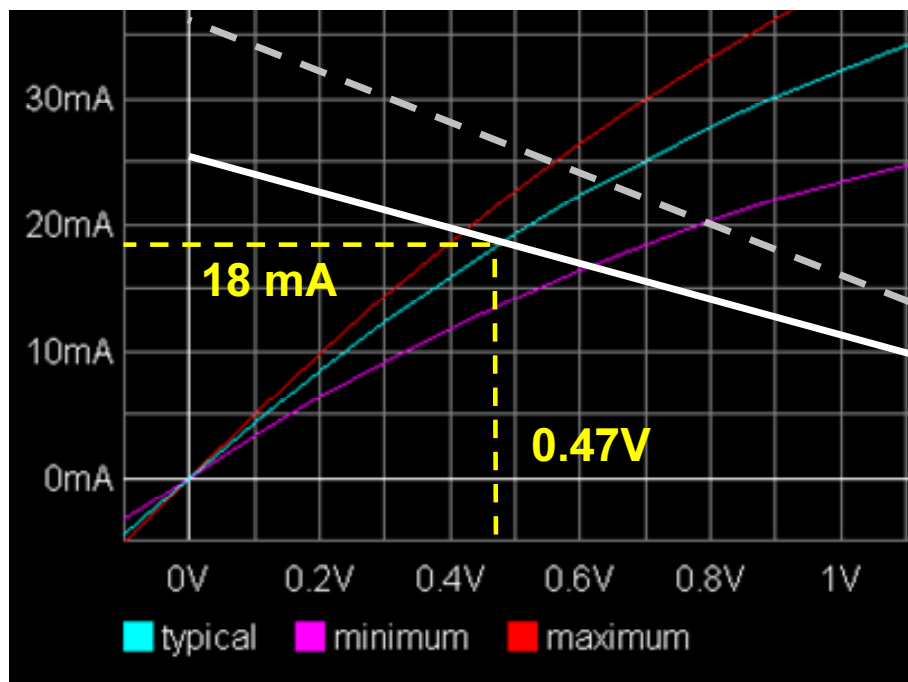
Updated Simulation Results



**Negative reflection
off driver's C_COMP**

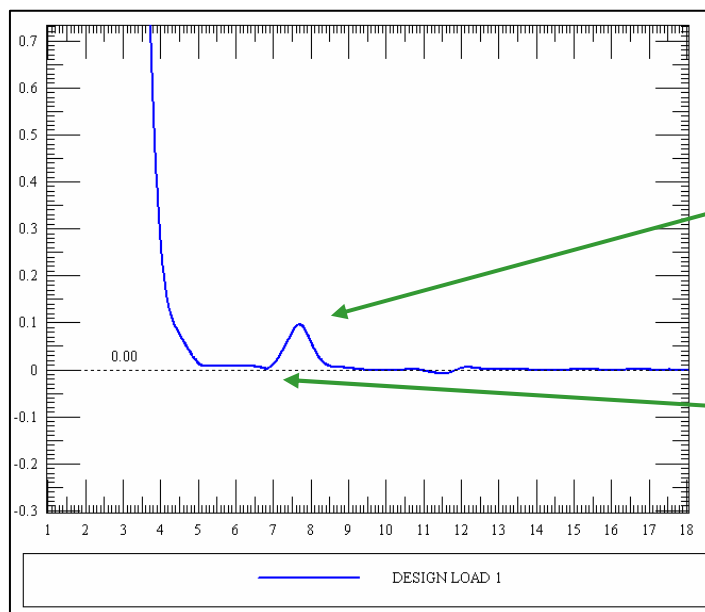
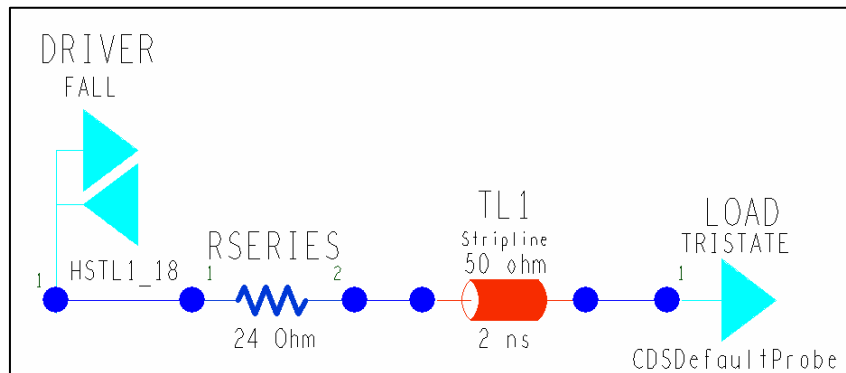
**Still slight overshoot;
25mV below GND**

Why Is There Still Overshoot?



- The series resistor changes the transistor's operating point
- Load line is now 72 (50 + 22) ohms to VDDQ
- If the V/I curve isn't linear between the new and old operating points, Z_{out} will change
- New $Z_{out} = 0.47V/18mA = 26$ ohms

Simulation Results For New Load Line

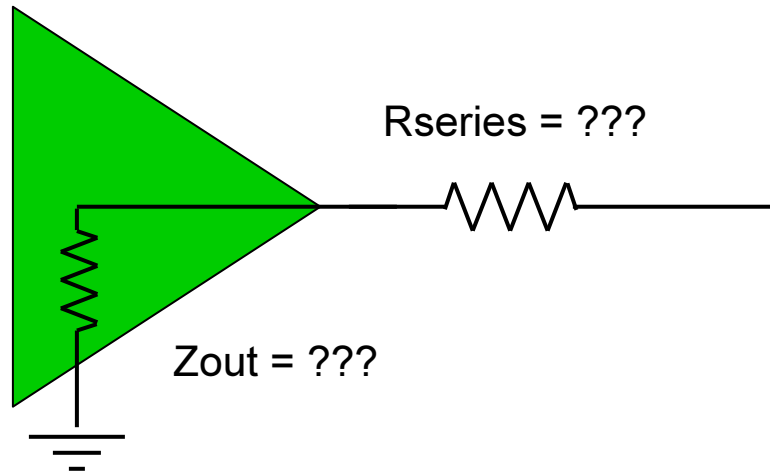


**Negative reflection
off driver's C_COMP**

**Overshoot is
basically gone**

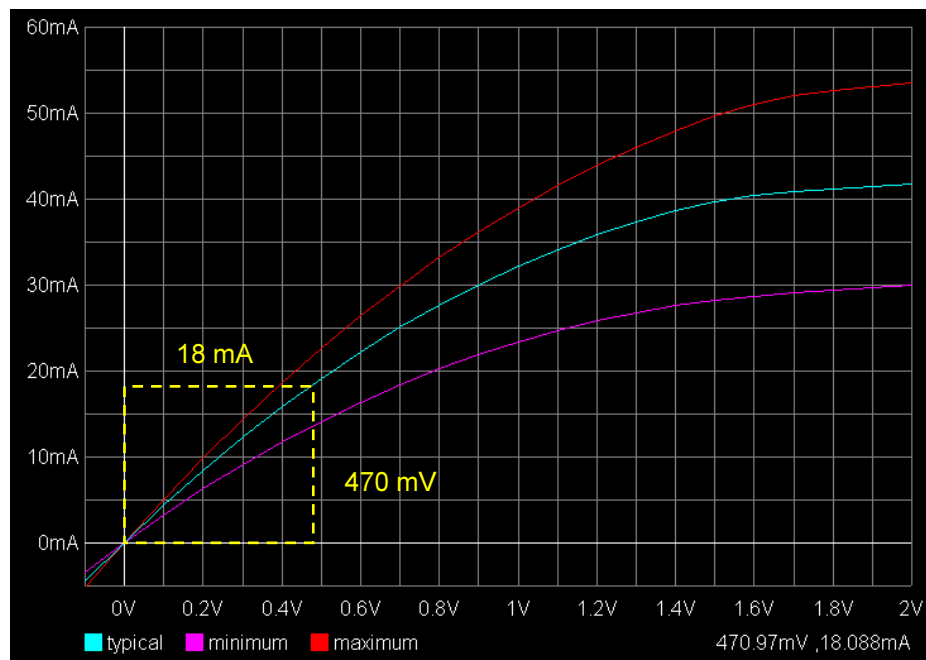
How Do We Determine Z_{out} and R_{series} ?

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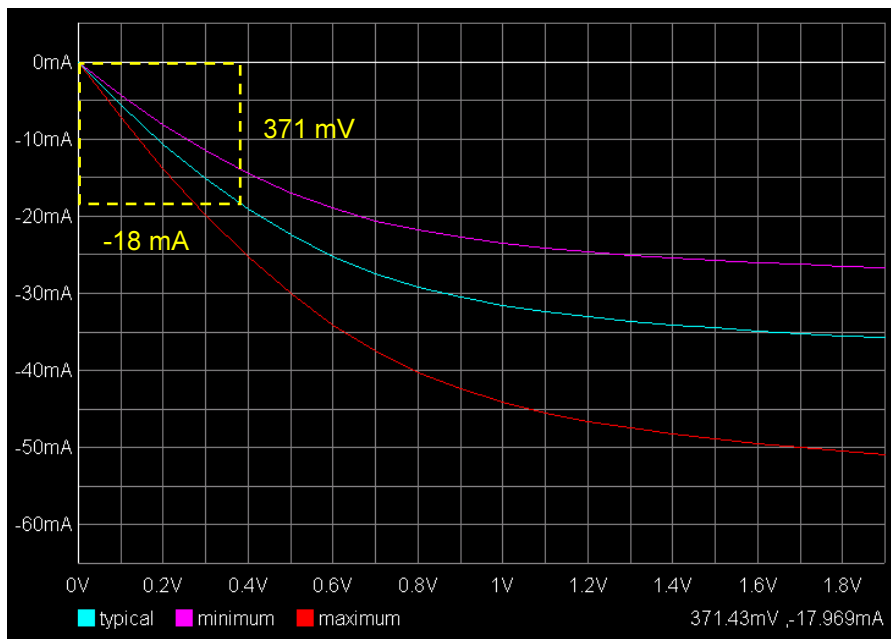
1. Determine ideal current from $I = V_{DDQ}/100$
2. Find corresponding current point on V/I curve
3. Compute $Z_{out,eff} = E_{curve}/I_{curve}$
4. Assign R_{series} such that $Z_{out,eff} + R_{series} = Z_0$

For Our 1.8V HSTL Buffer ...



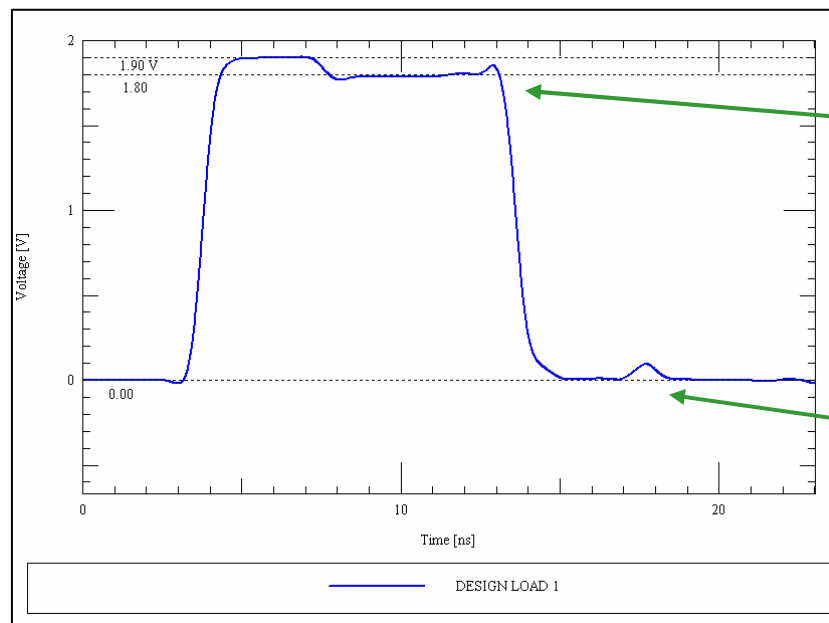
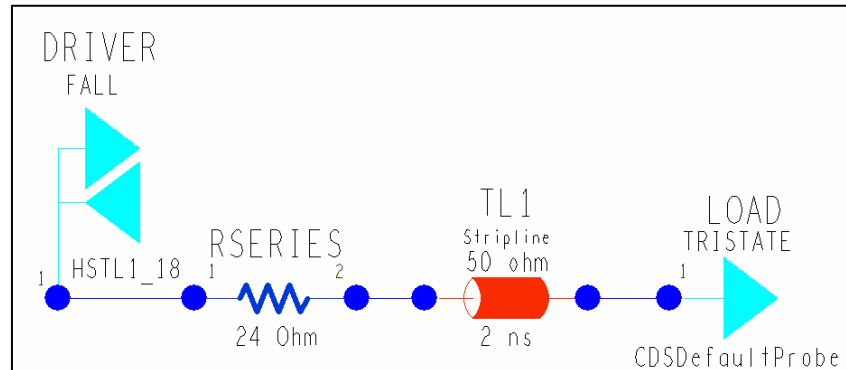
1. $I = 1.8V/100 = 18mA$
2. From the pulldown curve, $E=470mV$ at $I=18 mA$
3. $Z_{out,eff} = 0.47/0.018 = 26.1 \text{ ohms}$
4. $R_{series} = 23.9 \text{ ohms}$

Pullup Curves Work The Same Way



1. $I = 1.8V/100 = -18mA$
(IBIS convention)
2. From the pullup curve,
 $E=371mV$ at $I=-18 mA$
3. $Z_{out,eff} = 0.371/0.018$
 $= 20.6$ ohms
4. $R_{series} = 29.4$ ohms

Pullup/Pulldown Simulation Results



Overshoot on rising edge

R_{series} well matched for falling edge

Observations

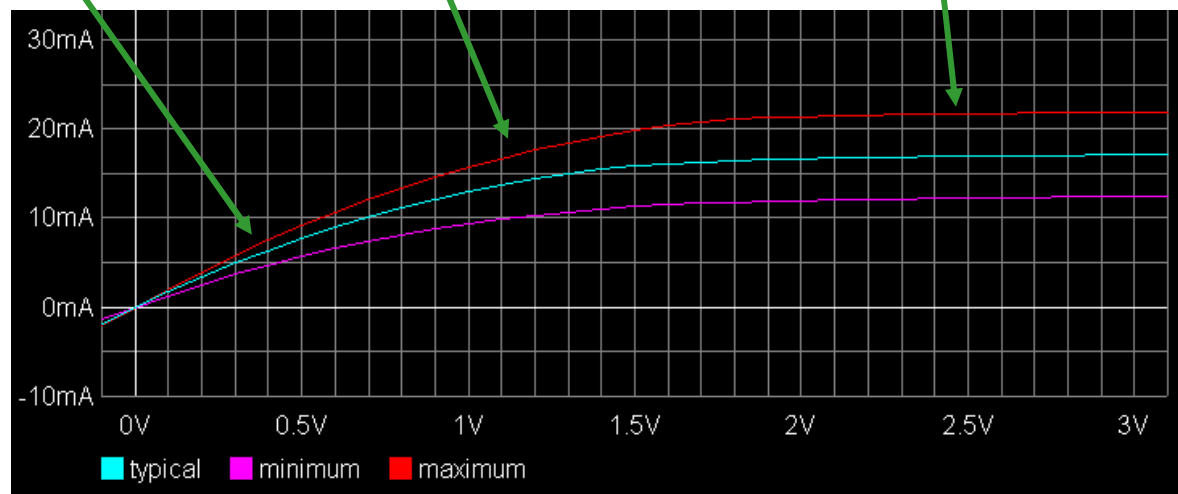
- This is a HSTL Class 1 buffer; we'd expect it to be designed for point to point operation without termination (50 ohm Z_{out})
- $Z_{out,eff}$ ranges from 21-26 ohms, requiring a series resistor to avoid overshoot
- Pullup/Pulldown are not well matched (21 vs. 26 ohms)
- This could either be a buffer design issue or a modeling issue

More On V/I Curves

Linear Region

Nonlinear Region

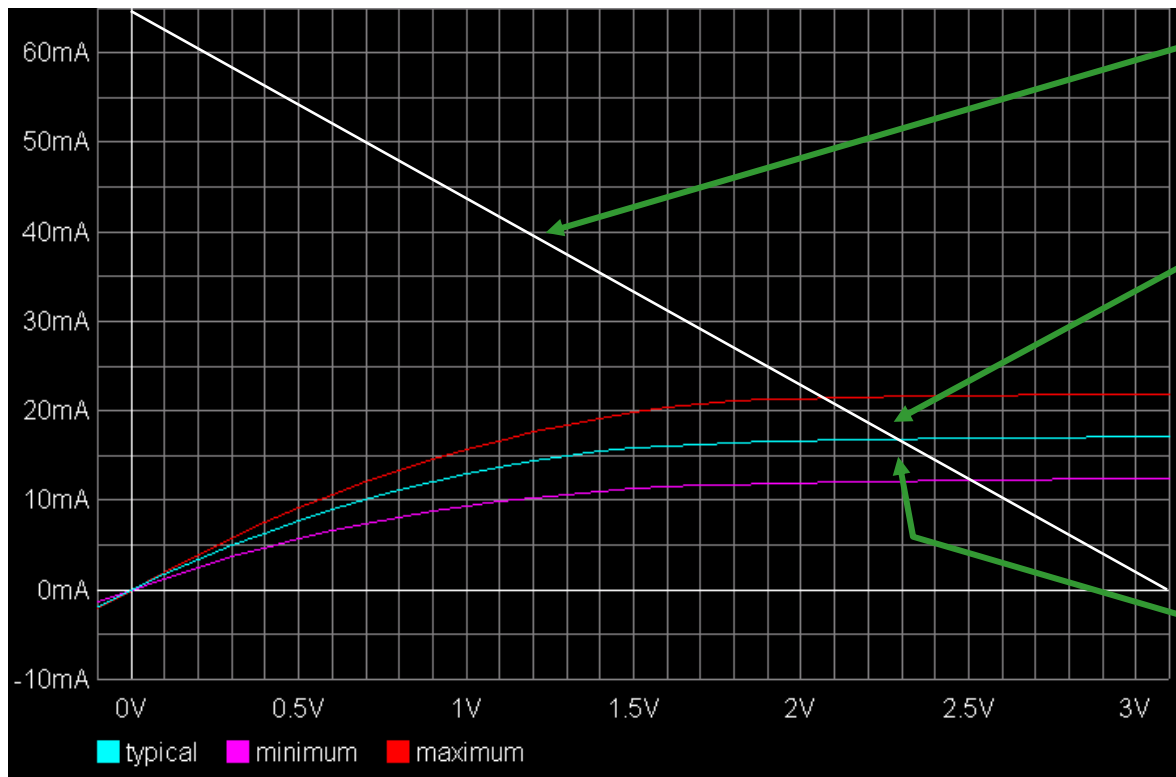
Saturated Region



- **Where the load line intersects the V/I curve says a lot about how the device will behave**

3.3V, 4mA LVTTTL Buffer Pulldown Curve

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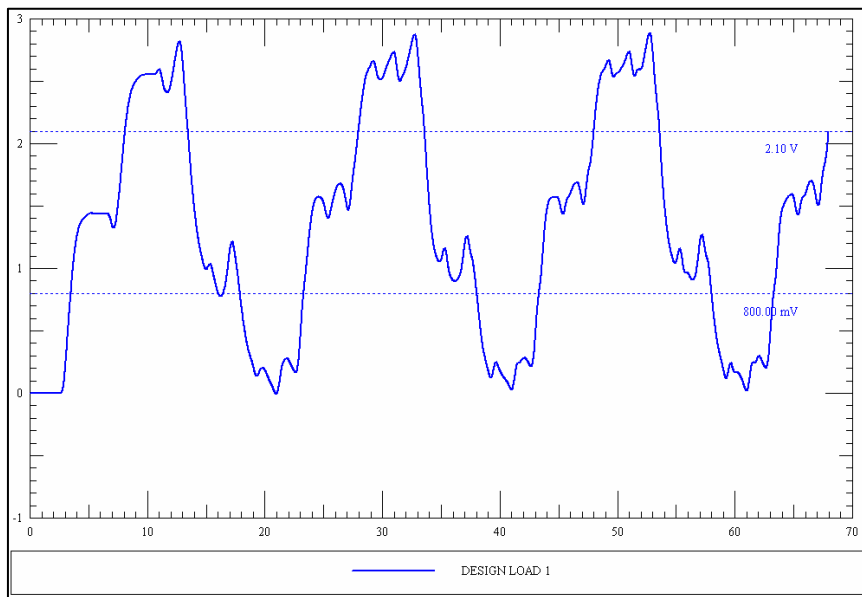
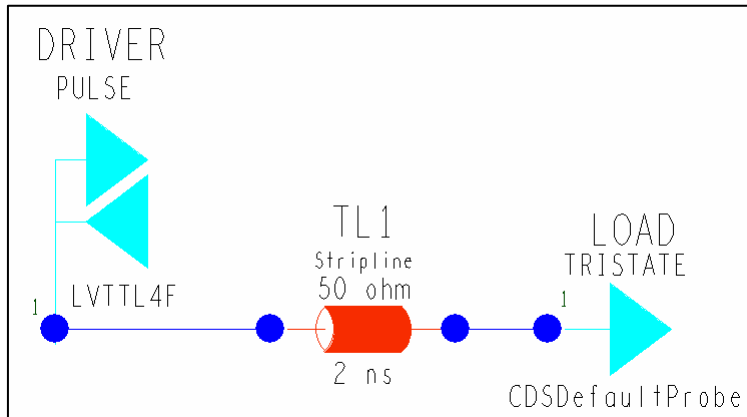
50 ohm, 3.3V
load line

Current at this
point determines
overshoot /
undershoot
at the receiver

The slope of the V/I
curve at this
point determines
how the driver
absorbs reflections

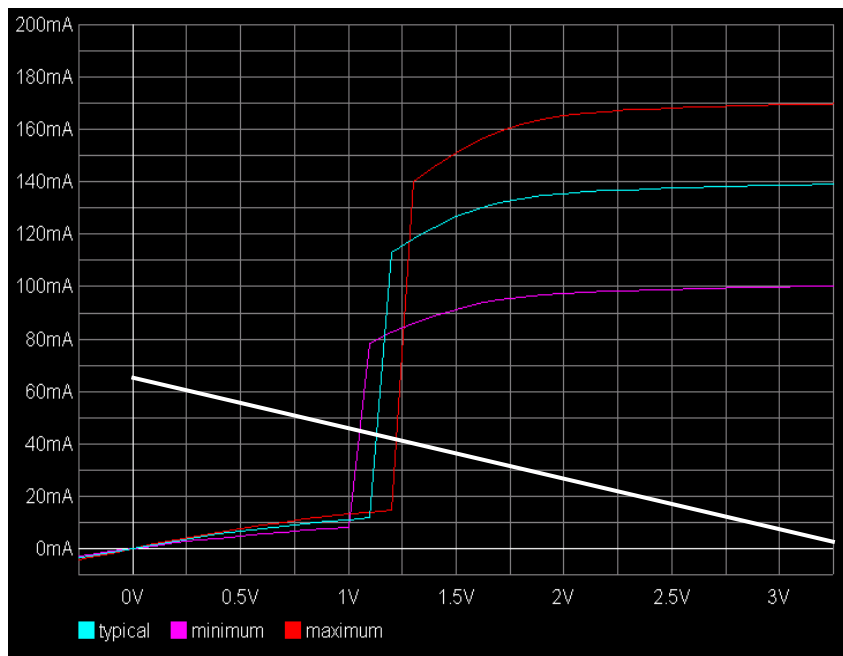
- This device can't drive a 50 ohm line; we need 30 mA, the output can only supply 17 mA

Simulation Results, 4mA Buffer



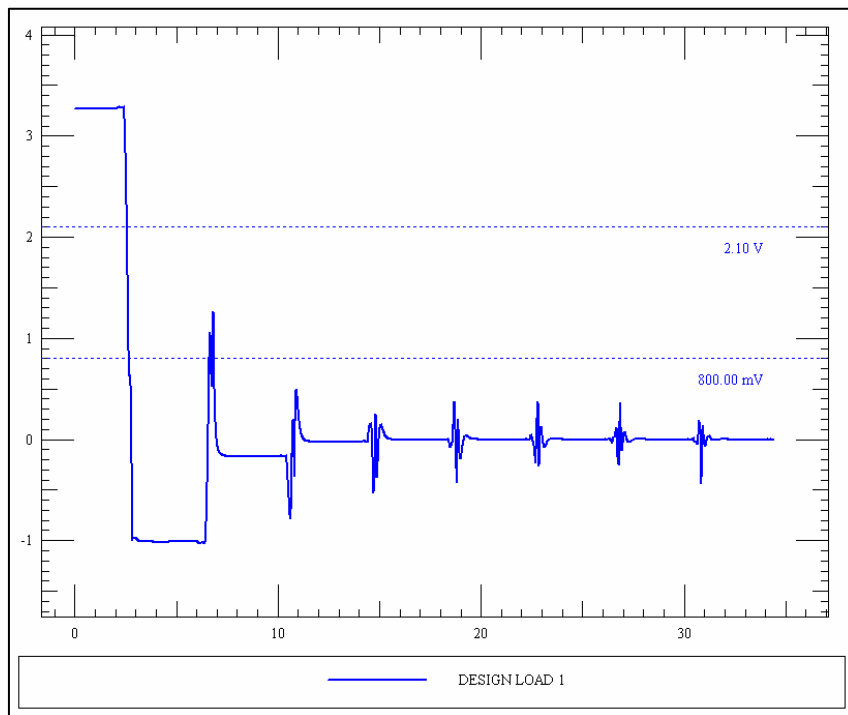
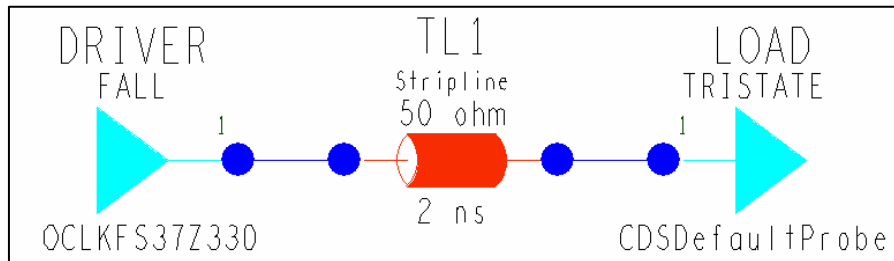
- **As expected, the driver cannot drive the line or adequately control the reflections**

3.3V Clock Output Buffer Pulldown



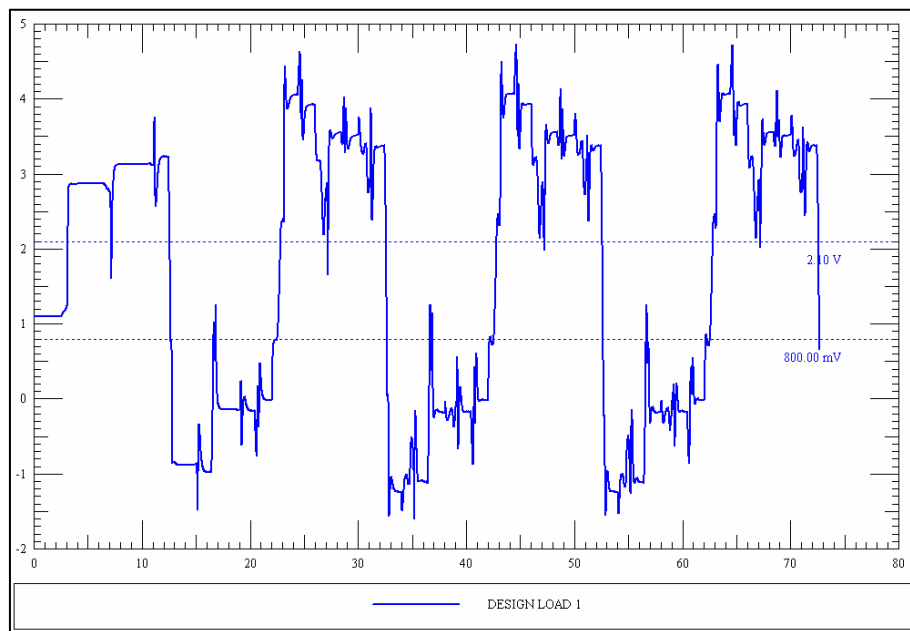
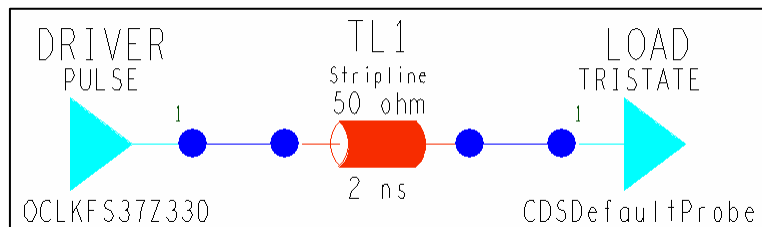
- Load line suggests buffer will drive about 42mA into a 50 ohm line; we only need 30mA
- Step voltage $E=IR$, $42 \text{ mA} * 50 \text{ ohms} = 2.1\text{V}$, so we expect about 900 mV overshoot
- Slope of V/I curve at load line is very high; expect very poor absorption of reflections by driver

Simulation Results – Falling Edge



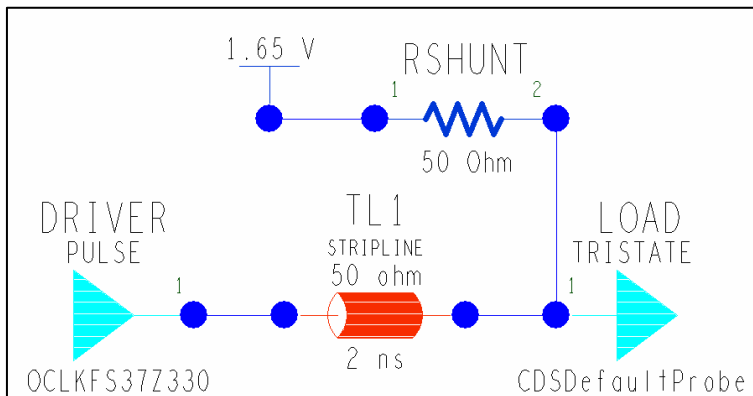
- **Overshoot slightly exceeds expectations**
- **“Ringing” occurs because of slope of V/I curve at the load line**

More Simulation Results ...

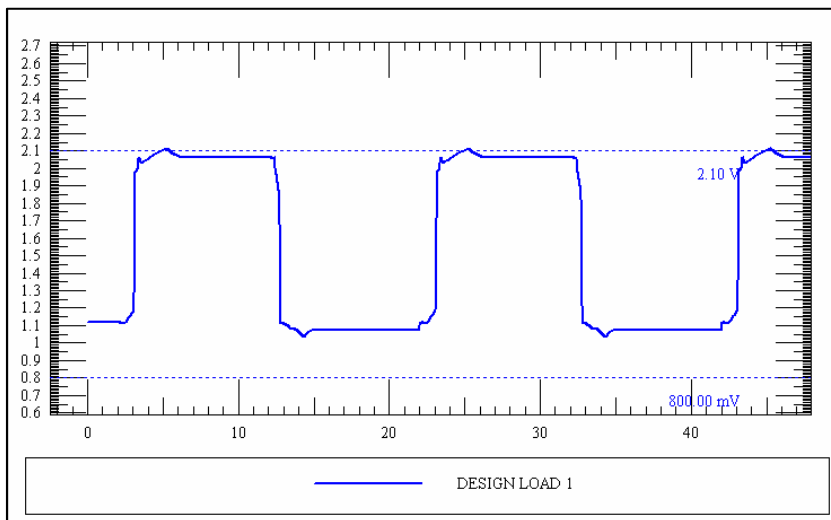


- “Ringing” amplifies over time; the model essentially spins out of control

Eliminate Reflections And ...



- **Ideal termination at the end of the line eliminates reflections off the driver**
- **Now we have a voltage threshold problem**
- **This may be a modeling problem anyway; should be investigated further**



Summary

- **Depending on the ratio of edge rate to line length, drivers can spend much of their time in “steady state” conditions**
- **“Steady state” behavior is driven by V/I curves**
- **Understanding the details behind V/I curve can provide valuable insight into**
 - **Buffer behavior**
 - **Model quality**
 - **Termination selection**

Yoda Says



- **Mind your V/I curves!**
 - Important, they are!
 - Save you, they can!