

## 3.2 Extracting Ramp Rate or V-T Waveform Data from Simulations

Simulations to obtain the ramp rate and/or V-T (output voltage versus time) tables are relatively straightforward. When modeling a CMOS or TTL buffer, for each simulation corner (minimum, typical, maximum), four V-T data sets are generally recommended. A special load is used for the purpose of model creation; we recommend the use of resistance loads. Note: This load is not the circuit load. The switching circuit conditions are described

in Section 3.2.2. Note that the specific load conditions may vary depending on the design of the buffer.

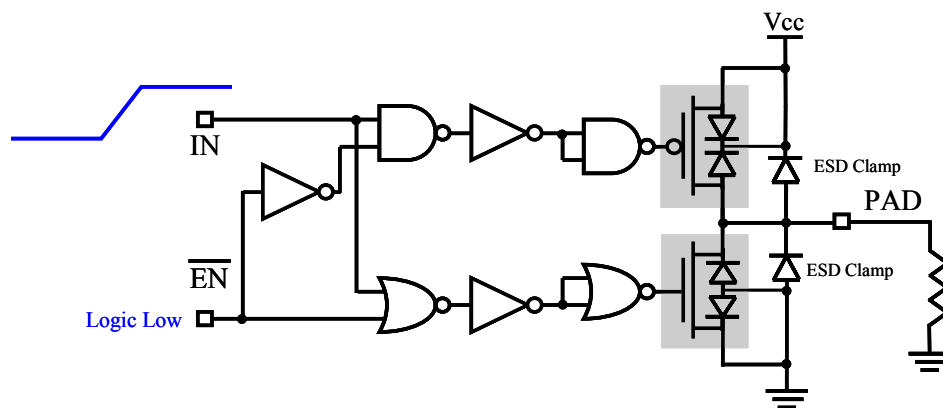
The ramp subparameters  $dV/dt_r$  and  $dV/dt_f$

(rising and falling  $dV$  and  $dt$ ) are extracted from the transitions where the device is “turning on” – switching to high against a low-voltage fixture and switching to low against a high-voltage fixture. The numbers  $dV$  and  $dt$  are not divided, since EDA tools may use  $dV$  and  $dt$  separately. Note that ramp data is required, and the V-T tables are strongly recommended. Further, be aware that the IBIS specification permits up to 100 waveforms to be included to describe buffer transitions, using a variety of loading conditions (see below).

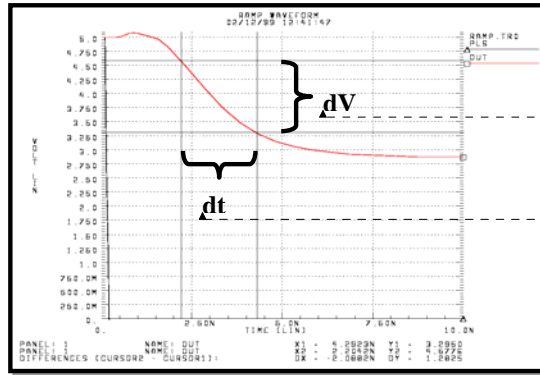
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### 3.2.1 Extracting Data for the [Ramp] Keyword

If the output switching (V-T) waveform of a buffer can be approximated by a linear ramp (i.e., the V-T waveform has no abrupt changes in shape, there are no “pedestals” in the waveform, etc.) then the V-T data may be reported as a rising and falling ramp data ( $dV$  and  $dt$ ) by using the [Ramp] keyword. Data for the [Ramp] keyword may be extracted using a simulation setup similar to that shown in Figure Error! No text of specified style in document..1 (a and b) below. In IBIS 1.1, switching information can only be represented through the [Ramp] keyword.



**Figure Error! No text of specified style in document..1 – a) Simulation Setup for Extracting Ramp Rate Information (Rising Edge Shown)**



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Figure part (b) Example of getting  $dV$  and  $dt$  from the 20% and 80% points in the simulation output.

Obtain rise and fall time data by setting the simulator for a transient analysis simulation. The control inputs of the buffer are set to enable the buffer outputs and a driving waveform is applied to the buffer core-side input. The slew rate of the input stimulus driving waveform should be appropriate to normal use of the buffer (i.e., the slew rate of the pre-driver that would normally drive the final output stage). Rising ramp rate data is obtained by placing a load resistance from the output to ground then stimulating the buffer so that the output switches from low to high. Falling ramp data is captured with the load resistor tied to Vcc. In general, a load resistance of 50 ohms is recommended, but this may not be appropriate in all cases. If the buffer does not have enough drive capability to make a significant output transition then a higher value of load resistance may be used, but this must be noted in the IBIS file (see the description of the [Ramp] keyword in the IBIS specification for details). For an open-drain or ECL/PECL buffer, measure the rise and fall times into the load resistor and voltage used by the manufacturer when specifying propagation delays. As with the I-V simulations, the package lead (L\_pin, R\_pin, C\_pin) parasitics must be removed. However, simulations should include C\_comp effects.

### 3.2.2 Extracting Data for the Rising and Falling Waveform Keywords

In IBIS versions 2.1 and above V-T data may be reported directly by using the [Rising Waveform] and [Falling Waveform] keywords. These two keywords are strongly recommended if the output switching waveform of the buffer is significantly non-linear (this is the case with most “controlled rise time” buffer designs). The use of these keywords is also indicated if the buffer incorporates a delay between the turning off of one output transistor and the turning on of the other.

When performing simulations to extract V-T data for the [Rising Waveform] and [Falling Waveform] keywords, a load resistor equal in value to a nominal transmission line impedance (such as 50 ohms) is used. Note that up to 100 V-T tables are permitted. If other load circuits are used, the resulting data should be stored as [Test Data] (see Section 5.5.8). By selecting the proper load(s) and termination voltage(s), the turn-on time, turn-off time (and overlap between the two) of the pullup and pulldown stages of the buffer can be isolated in simulation and a more accurate behavioral model constructed.

A few recommended loads and waveforms are listed in Table **Error! No text of specified style in document..1** below.

Technology	# of Waveforms	Load Circuit and Waveform	Notes
Standard Push/Pull – CMOS	4	1R + 1F driving 50 Ω to Vcc 1R + 1F driving 50 Ω to GND	1
Open-drain/collector– CMOS, TTL and GTL	2	1R + 1F into manufacturer’s suggested pullup resistor termination and voltage	1, 2
Open-source/emitter – CMOS and TTL	2	1R + 1F into manufacturer’s suggested pulldown resistor termination and voltage	1, 2
ECL	2	1R + 1F into manufacturer’s suggested pulldown resistor termination and voltage	3

1. 1R = one rising waveform, 1F = one falling waveform
2. If termination resistor is > 100 ohms, include 1R + 1F driving 50 ohms to termination voltage
3. A load of 50 ohms to a voltage of Vcc – 2 is a fixture typically recommended by manufacturers

**Table Error! No text of specified style in document..1 – Recommended Load Circuits and Waveforms for V-T Data Extraction**

**Note:**

Be aware that not all EDA tool vendors’ simulation software may use all the V-T tables provided in the model. If in doubt, check with your EDA tool vendor.

In many cases, particularly for buffers with fast output transitions, the most appropriate load is a resistive value corresponding to the impedance of the system transmission lines the buffer will drive. For example, a buffer intended for use in a 60 Ω system may best be modeled using a 60 Ω load (R\_fixture).

While supported by the IBIS version 2.1 specification and later versions, the use of reactive elements as V-T table loads is not recommended. A resistive load should be used wherever possible.

As with the simulations for ramp rate, the slew rate of the internal driving waveform should be appropriate to the normal use of the device. For meaningful results, all of the above rising and falling waveforms should be taken with the package parameters (R\_pin, L\_pin and C\_pin or R\_pkg, L\_pkg and C\_pkg) and fixture reactive elements (L\_fixture and C\_fixture) set to zero. As noted in the IBIS specification, all rising and falling waveforms should be time-correlated. In other words, the data in each of the rising edge waveform tables must be entered with respect to a common reference time point on the input waveform used to stimulate the buffer. The data in each of the falling edge waveforms must be time-correlated in a similar manner.

Finally, some buffers may show slightly different rising and falling edge characteristics depending on how much time the buffer has had to settle from a previous output transition. Some projects may ask that the model creator extract ramp or V-T data from the second or third output transition in a series. Note, however, that all V-T table data should be extracted over a duration long enough to ensure steady-state DC behavior at the start and at the end of the data set. In some cases, this may require simulating buffer performance for a significant period before collecting transition data, in order to ensure any logic associated with the driver is in a known DC state. Note that IBIS 4.0 and higher requires that all V-T tables be time correlated; that is, all tables use the same time reference. Typically, one V-T simulation will have TIME=0 at the start of the input transition for which the V-T data is extracted; this means that the Time data must be shifted for those tables where you are not using the first transition.

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### **3.2.3 Minimum Time Step**

As a rule of thumb, set the minimum time step to maximize the number of data points in the rising and falling V-T tables within the limits of the IBIS specification. The V-T waveform tables can contain no more than 100 points under IBIS version 3.2. IBIS version 4.0 permits up to 1000 points per V-T table).