Whose fault is it?

Our schedule is slipping because your **hardware** design is unstable!

Our schedule is slipping because your **software** did not take into account all of my hardware features!

- How do we going to maximize power savings if this is how we work together?
AGENDA

- Why is power management important?
- Introduction to power management
  - A System level issue
  - The business context
  - Power Optimization at every level
- Nucleus Power Manager
  - Power Model
  - Peripheral Power Management
  - Core Power Management
- Next Steps and External loop
The first cell phones made phone calls. Modern 3G Cell phones also make phone calls, and then some… Text, Camera, Email, Webrowser, Email client, GPS, games …
Specific Energy: the ratio of energy delivered by the battery to the weight of the battery measured in watt hours per kilogram (wh/kg)

Battery technology is not keeping up with the demand for more functionality
Power Management
For Portable Consumer Electronic Devices

- Battery Life
  - Maximize Battery Life
  - Minimize Size, Weight and Capacity
What is the problem?
Power Generation – Worldwide

Power Generation – Worldwide

- **Oil**: 37%
- **Coal**: 25%
- **Gas**: 23%
- **Nuclear**: 6%
- **Biomass**: 4%
- **Hydro**: 3%
- **Solar heat**: 0.5%
- **Wind**: 0.3%
- **Geothermal**: 0.2%
- **Biofuels**: 0.2%
- **Solar photovoltaic**: 0.04%

*Source: Renewables, Global Status Report, 2006 update; wiki - Omegatron*
Temperatures over past 2000 years

Source: www.globalwarmingart.com; Robert A. Rohde
Power Management
For Portable Consumer Electronic Devices

- Global Warming
  - Not just Set top boxes
  - Charging the battery from the Power Grid
Electricity consumed by US

- 11% of US household energy doubled in last 10 years
  - ~100 million kilowatthours

Government turns up the heat on consumer electronics; Electronic Business; 1/30/2007
http://www.eia.doe.gov/emeu/aer/eh/frame.html
Energy Star Requirements for Charging

Criteria for Active Mode
- Output Power (Pno) Minimum Average Efficiency in Active Mode
  - 0 to <= 1 watt >= 0.49 * Pno
  - > 1 to <= 49 watts >= [0.09 * Ln (Pno)] + 0.49
  - > 49 watts >= 0.84

Criteria for No-Load Mode
- Output Power (Pno) Maximum Power in No-Load
  - 0 to < 10 watts <= 0.5 watts
  - >= 10 to <= 250 watts <= 0.75 watts
Power Optimization at Every Level

- **SOC Physical**
  - Si Materials, Si Device Design, Device selection (gate choice), Place and Route, Power Gating (island), Back bias schemes (reduce leakage)

- **SOC Gate Level:**
  - Clock Gating, Clock tree synthesis

- **SOC Register Transfer Level:**
  - Sequential and combinatorial Clock gating

- **HW System Level:**
  - Processor choice, Bus choice, Memory Architecture
  - HW / SW choice for implementation

- **SW Level**
  - Control processor low power modes
  - Algorithmic performance
  - Optimize memory performance
  - Multicore utilization (thread management)
A System Level Issue

Power Management is a system level issue involving:

- **Peripherals**
  - Off chip peripheral such as LCD backlight, touch panel, camera, memory, SD/MMC controller...but also companion chip such as IPU, Wireless or cellular baseband
  - On-Chip peripherals such as bus controllers, memory controller, MultiMedia acceleration

- **Core**
  - Frequency (and voltage)
  - Low power modes

- **The « system » itself:**
  - The operating mode currently active
  - The data currently being processed

- **The Tools**
  - Power optimized code

Each item in this list represents an opportunity for system optimization and power consumption reduction.
“Timing Closure” has been the primary focus for SOC designers over the past 2 decades

- Design tools that specifically target timing closure have generated hundreds of millions, if not billions of dollars of revenue over the history

“Power Optimization” has become the next holy grail in HW design

- The market for HW power design tools exceeds $100M today, yet the biggest opportunities for power optimization are in the SW layer

Low Power design is a leading business driver for all electronic concerns
Power Management

Enabling longer battery life!

System Software Interfaces

- WiFi Driver
- LCD/Keypad Driver
- File Driver
- USB Driver

ARM

Power Mgt.
Power Management

Power Manager UI Control Demonstration

- Touch Panel
- LCD
- Backlight
- Keypad
Power Management

Power Manger UI Control Demonstration

Initialization

Initialize technical power domains
Creates associations as functional domains
Initiates the states and respective drivers

UI Functional Domain 1

Technical Domain 1

- LCD
- Touch Panel

Technical Domain 2

- Backlight

Technical Domain 3

- Keypad
- ...
Power Management

Power Manager UI Control Demonstration

- **Initialization**
  - Initialize technical power domains
  - Creates associations as functional domains
  - Initiates the states and respective drivers

- **Touch Panel used**
  - Reset Timer on UI functional domain

**UI Functional Domain 1**

- **Technical Domain 1**
  - LCD
  - Touch Panel

- **Technical Domain 2**
  - Backlight

- **Technical Domain 3**
  - Keypad
  - ...
Power Management

Power Manager UI Control Demonstration

- Initialize technical power domains
- Creates associations as functional domains
- Initiates the states and respective drivers

- Touch Panel used
- Reset Timer on UI functional domain
- Backlight to 50%

UI Functional Domain 1

- Technical Domain 1
  - LCD
  - Touch Panel

- Technical Domain 2
  - Backlight

- Technical Domain 3
  - Keypad
  -...

Mentor Graphics Confidential Information
Power Management

Power Manager UI Control Demonstration

- **Initialization**
  - Initialize technical power domains
  - Creates associations as functional domains
  - Initiates the states and respective drivers

- **Touch Panel used**

- **Timeout Event**
  - Reset Timer on UI functional domain

  - Backlight to 50%

  - Backlight/LCD and Touch Panel to OFF
  - Functional Domain 1 OFF
  - Functional Domain 2 OFF

UI Functional Domain 1

- **Technical Domain 1**
  - LCD
  - Touch Panel

- **Technical Domain 2**
  - Backlight

- **Technical Domain 3**
  - Keypad

...
Power Management

Power Manager UI Control Demonstration

Initialization

- Initialize technical power domains
- Creates associations as functional domains
- Initiates the states and respective drivers

Keypad Event

- Functional Domain 1 ON
- Reinitialize LCD
- Reinitialize Touchpanel
- Functional Domain 2 ON
- Backlight ON 100%

Touch Panel used

- Reset Timer on UI functional domain

Timeout Event

- Backlight to 50%
- Backlight/LCD and Touch Panel to OFF
- Functional Domain 1 OFF
- Functional Domain 2 OFF

Timeout Event

UI Functional Domain 1

- Technical Domain 1
  - LCD
  - Touch Panel

- Technical Domain 2
  - Backlight

- Technical Domain 3
  - Keypad
  - ...
Power Management State Machine

Diagram showing states: ON 100%, OFF 0%, STANDBY 25%, SLEEP 50%, IDLE 75%

Transitions:
- B/E/T: Battery/Event/Timer
- B/T: Battery/Timer
- E: Event
Reactive Power Management

Current draw from User Interface

- Initialize the system
- LCD ON / Backlight ON
- Inactivity Timer
- Touchpanel Event
- System on halted

Seconds

Current draw from User Interface
Power Efficiency

Speed and Performance variance as process nodes decrease

Source: common platform conference Energy Aware Multi-Processing with ARM Cortex-A9 MPCore

Decreasing Gate width

- Increases performance
- Initially decreased power
- Smaller geometry's hinder power savings due to both static gate leakage and increased frequency
Power Consumption

For Portable Consumer Electronic Devices

Two variables that can save power

- Frequency (only affects the dynamic piece)
- Voltage (can be decreased if Frequency is also decreased)

\[ CV^2 f + V I_{\text{leak}} \]
DVFS – Triangle Utilization Pattern
PMP Application with and without Power Management
Results PMP Sinewave 220Hz

Sinewave 71db

milliamps

1 202 403 604 805 1006 1207 1408 1609 1810 2011 2212 2413 2614 2815 3016 3217 3418 3619 3820 4021 4222 4423 4624 4825 5026

Linux
Nucleus
Next Generation Embedded Systems

System-Wide

Hardware
- CPU Control of sleep modes
- Dynamic Frequency and Voltage Scaling (DVFS)
- Dynamic Process Temperature Compensation (DPTC)
- Independent Peripheral Clock Gating
- Peripheral Low Power Modes

Software
- Power Aware Drivers
- DVFS enabled control of CPU
- Battery Charging Control
- Reactive Power Management
  - Use it or lose it.
  - Control power aware hardware.
- Proactive Power Management
  - Predict what the power use needs are before you need them.
Conclusion: Power Management
A System Perspective

- Are not just for battery operated devices
- Must consider the whole life cycle of how the device is utilized
- Must consider the whole infrastructure surrounding the system
- The HW must provide power saving IPs
- The OS must enable power saving techniques
- The system integrator must use them

This is our challenge for the next generation of embedded systems. The next generation depends on us.
Questions
Thanks!

www.mentor.com/embedded
System Example

System Attributes
- Set Top Box
- Hardrive to store movies
- 10 new HD movies per week
- Uses broadcast subcarrier
- Always on
- Has USB and Ethernet
- Runs COTS OS
- User can select any movie of the 100 stored on STB.
- Oldest movies are deleted
System Example

System Attributes

- Set Top Box
- Hardrive to store movies
- 10 new HD movies per week
- Uses Internet multi-cast
- Has back-channel
- User can select any movie of the 100 stored on STB.
- Oldest movies are deleted
- Only on for downloads and on demand for viewing movies
Thanks!

www.mentor.com/embedded
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  - Low power modes

- **The « system » itself:**
  - The operating mode currently active (the use case in progress)
  - The data currently being processed

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Each item in this list represents an opportunity for system optimization and power consumption reduction.
HW Power Optimization

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Power Model

The power model represents the system power states.

The Power manager moves from one mode to the other based on events such as battery level, timer, user event, peripheral notification, interrupt etc.. Each transition is attached a dedicated processing. Such processing can be simple (register operation) or complex (frequency scaling, system shut down).

Battery powered systems always have a more or less...
Peripheral Power Management

Peripheral power management is critical as peripherals have a large contribution to the overall power consumption. They deserve special attention.

In most cases, it is possible to manage the peripheral power modes independently.
Peripheral Power Management (cont.)

Each peripheral is associated with its own power model, implemented as state machine just like the system power model.

All the power-enabled peripherals then report their status to the system power model where system level decisions can be made.

Not all the peripherals are independant from the logical or functional view point.
Core Power Management

The power consumption of CMOS digital circuits is proportional to the frequency and to the square of the core supply voltage.

The static contribution is very small (<figure needed>), so the focus is on the dynamic part: $CV^2f$

The system does not require 100% of the processing power all the time. So, modern processors offer means to adapt the processing capacity to the system demand:

- DVFS (during processing)
- Low power modes (during inactivity)
DVFS management is about setting the most appropriate CPU function point, based on the system need.

The challenge is to be able to evaluate and/or predict the system need at a particular point in time. Multiple policies can be defined with different levels of complexity.

We will start with a « minimum idle time policy » that implements a negative feedback loop.

Note: Voltage and Frequency are linked: not all frequency are possible at a particular voltage. The processor has actually a discrete number of function point available: e.g. for PXA270: (0.9, 104), (1.15, 208).
Low Power Modes

- Low power mode management is about placing the core processor into the lowest possible power mode when there is no processing demand. Modern processors have multiple low power modes: Idle, Stand-by, Sleep, Deep-Sleep

- The challenge is to be able to set the ‘alarm clock’ so that no event is missed. Bearing in mind that wake up time can be long.

PXA270 low power modes

- Running mode:
  - 925mW @ 625MHz
  - 44mW at 13MHz.

- IDLE mode
  - 260mW @ 624MHz
  - 8.5mW at 13MHz.
  - It takes 1usec to enter / exit this mode

- Stand By:
  - 1.7 mW.
  - It takes up to 11msec to exit this mode.

- Sleep Mode
  - 0.16mW
  - It takes up to 136msec to exit this mode.

- Deep Sleep Mode
  - It consumes 0.1 mW.
  - It takes up to 261msec to exit this mode.
Next Steps and External Loop

- Power management agent takes more inputs and output to more component
- The external loop optimizes the memory mapping and code efficiency
SUMMARY

- We are committed to power saving.

- The first implementation of our power framework will have
  - Peripheral management
  - DVFS with a ‘minimal idle thread’ policy
  - Simple low power modes management

- Moving forward, the framework will have
  - more policies, fine grain control over the peripherals, more kernel awareness, smart low power modes management.
  - We also are looking at providing the user with power profile integrated into our tool offering
Thank you!

Questions?
Background
ST Low Power Solutions Roadmap

System/SW
- SystemC TLM Platform
- Power Control Insertion
- Power Back-Annotation from HLS into TLM

RTL
- RTL Power Estimation
- RTL Power Optimization
- Static Power Checking
- Design Techniques
  - Low Power FFs
  - Power Gating
  - Source Biasing
  - Dual-voltage SRAMs
  - Power distribution
  - Low-VDD Retention
  - Forward/Reverse Body Biasing

Tx
- Design Challenges at 45nm and below

2006-7: 65-45nm
2008: 45nm
2008-9: 45-32nm

Higher Accuracy
Raise Abstraction
In 2004-2006 a Cisco business unit shipped 5 Million Systems With a total of 500 Megawatts Usage

If these 5 Million Systems had shipped with 1 Watt LESS each…

5 Megawatts of Power would not have shipped
16 Million KWatt Hours saved per Year
$3.8-$7 Million Electrical Expense
31 K Metric Tons CO₂ eliminated from Atmosphere
Double for Cooling & Auxiliary (C & A)

Equivalent to taking 12,000 Cars off the Road…
Big Volume Amplifies Small Gains!

Source: Cisco Lynelle McKay, Senior VP and General Manager, Networking & Computing Systems Group, a Cisco Business Unit
50 percent of the cost of a data center is associated with expensive power and cooling equipment.

Source: Power Architect development Conference, Steve Carlson

Cost of Power Cooling

The hot and cold of power and cooling - HP June 2006
“Earlier this month the giant chip maker [Intel] pushed up the date to June 26 in an attempt to take back momentum from rival AMD, which has gained market share over the past couple of years based on the strength of the performance-per-watt capabilities of its Opteron processors.”

Source: Will Intel Get Its Groove Back with 'Woodcrest'?
BASELINE, June 2006, by Jeffrey Burt

Intel Xeon 5160 CPU Dual-Core
3.0GHz, 4 MB L2 shared,

AMD Opteron 2216HE CPU, Dual-Core, 2.4GHz, 2MB L2 Cache

Source: AMD Processor/Memory Comparison of Intel and AMD product. Energy includes power input & cooling. Power Utility cost: $0.10/KW-hr. Publicly available processor & chipset specifications. The examples contained herein are intended for informational purposes only. Other factors will affect real-world power consumption and cost.
Power is a Key Competitive Advantage

Dual-Core Intel Xeon MP (‘Paxville MP’)
- 692 watts for processors (173w MAX POWER)
- 92.4 watts for chipset, 140.8W for memory
$1,297 per/year (1 server)
$648,380 per/year (500 servers)

Dual-Core AMD Opteron™ 8000 series
- 380 watts for processors (95w MAX POWER)
- 24 watts for chipset, 140.8W for memory
$764 per/year (1 server)
$381,796 per/year (500 servers)

Source: AMD Processor/Memory Comparison of Intel and AMD products. Energy includes power input & cooling, Power Utility cost: $0.10/KW-hr, Publicly available processor & chipset specifications. The examples contained herein are intended for informational purposes only. Other factors will affect real-world power consumption and cost.
Power Impacts Business!

iPhone Battery Improved; Apple Stock Up

There were announcements this morning that Apple had addressed two issues with the iPhone - the non-user-replaceable battery had its battery life runtimes increased and the covering for the touchscreen has been changed from a plastic material to glass. Apple’s stock was up almost 4% on the day due to that news.

= ~$3B

In one day

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How to Reduce Power?

Physical Optimization Methods

- Limited Optimization Margins

<table>
<thead>
<tr>
<th>Method</th>
<th>Static Power</th>
<th>Dynamic Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area Optimizations</td>
<td>10%</td>
<td>10%</td>
</tr>
<tr>
<td>Clock Gating</td>
<td></td>
<td>20%</td>
</tr>
<tr>
<td>Multiple Supply Voltages (MSV)</td>
<td>20%</td>
<td>20%</td>
</tr>
<tr>
<td>Shut Down Power Modes</td>
<td>~50%</td>
<td>0%</td>
</tr>
<tr>
<td>A/DVFS (Adaptive/Dynamic Voltage Frequency scaling)</td>
<td>~10%</td>
<td>&gt;40%</td>
</tr>
<tr>
<td>SW [User Experience]</td>
<td></td>
<td>&gt;60%</td>
</tr>
</tbody>
</table>

Source: Institute of Electronic Design Automation, Technical University of Munich

Nikkei Electronics Asia -- September 2005
Robert Aitken, George Kuo, and Ed Wan EE Times

Source: Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, Illinois, USA