Integrity Must Be Integral

Daily Life of a SI Guy in EDA

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Outline

• Long-term impacts of daily decisions
• Considerations involved in solving a problem with right efforts at the right place
• Case studies
  ▪ Crosstalk
  ▪ Power
  ▪ Power supply noise
• A glance into the future
Physical Problem Solving in EDA

- A physical phenomenon gets noticed due to its impact on performance, cost, competitiveness, or reliability
- “How serious is this problem on MY design?”
- “Well it’s a concern but not too bad. How can we fix it after design is complete?”
- “3,000 violations? It’s going to take forever! Can’t you prevent it?”
  - “Of course everything important before still needs to be taken care of.”
  - “Oh, by the way I can’t afford tape-out delay. Do it smart and fast.”
Pressure on EDA is ON

• Software Infrastructure
  ▪ Database
  ▪ Runtime data model
  ▪ User interface

• Flow
  ▪ Library
  ▪ Analysis engines
  ▪ Implementation engines
  ▪ Sign-off tool
  ▪ Trade-off’s
  ▪ Last touches – ECO
Now do the above 4 times!

Timing

Crosstalk

Power

Voltage Drop & Reliability

“Did I tell you the process variation problem that’s been bothering me?”

“It would be really nice if you can somehow analyze chip performance including the core, I/O, packaging and board all together.”
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Different Effort Levels: Point to Flow

- Some problems can be solved with incremental changes to existing system
  - HCE, Signal EM, Power
- Some problems can be addressed by making information available
  - Timing, Crosstalk, Power
- Some problems challenge fundamentals of a software system
  - Power (multi-Vdd, multi-mode)
- Some problems challenge fundamentals of design flow
  - Crosstalk, Resistive Shielding
Uneven Effort Levels

- Case 1: Implementation Engines
  - Signal EM, HCE
- Case 2: Analysis Engines
  - Voltage drop
Database Characteristics

- Representation by
  - View (timing, power, SI)
  - Abstraction level (transistor, cell, RTL)
  - Hierarchy
- Object Relationship and Maintenance
- Update mechanism
  - Incremental
  - Batch
- Flexibility
  - In-memory vs. disk I/O
  - Query
Runtime Data Model

- Mapping mechanism with database
- Capacity vs. reference to database
- Native vs. subscription based costing
- Flow representation and interface between sub-systems
User Interface

- Mapping mechanism with database
- Text vs. graphics
- Scripting vs. forms
- Details vs. speed
- Ease-to-query vs. capacity
- Editing, design change and legalization
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Crosstalk: Why is it so Hard?

- Introduces spatial correlation among signals
  - Routing pattern
  - Driving strength
  - Clock domain
  - Timing window
  - Logic correlation

- Design complexity goes from $O(N)$ to $O(N^2)$

- Necessitates explicit consideration of nonlinear behavior of digital circuits
  - Waveform vs. ramp approximation
  - Noise propagation
Crosstalk: Why is it so Hard? (cont’d)

• Adds complexities to hierarchical design flow
  ▪ Macro model needs to carry more attributes
    • Physical: crosstalk model parameters of boundary nets
    • Timing: uncertainty due to crosstalk
  ▪ Additional physical and timing constraints
• Pessimism removal is challenging yet must be done
  ▪ Logic correlation: deterministic vs. probabilistic
  ▪ Timing window: accuracy vs. data volume
Crosstalk-aware Design Flow

Placement w/ HFN or w/o (congestion removal)

Post Placement Opt

Clock Tree Synthesis

Global Route/Track Assign
SI prevention

Post Route Opt

Sign-off Analysis & ECO

Crosstalk Prevention
- Placement based prevention through slew balancing and congestion removal
- GR/TA prevention through routing density, length, and layer control
- Routing based prevention for clock

Crosstalk Fixing
- Topology based optimization considering crosstalk

Crosstalk ECO
- Sign-off tool generates constraints and ECO deck

*Optional step when HFN is not done in PC
Crosstalk: Status

• Flow is there but a lot of work remain to be done
  ▪ No single step can solve crosstalk alone. Divide-and-conquer is key
  ▪ Balance aggressiveness in crosstalk prevention / correction with timing, power, and area
  ▪ Balance sophistication of crosstalk model with runtime, memory, and accuracy of input parameters
  ▪ Correlation with sign-off tool needs to be pursued but not too hard
  ▪ Efficient ECO flow is critical to closure
Power

• Can power be analyzed rather than measured?
  ▪ Will there ever be power “sign-off?”

• Implications of power management techniques on power analysis

• Power management has associated costs
Power Analysis Status

- Power sign-off requires efficient ways of finding
  - Average power
  - Worst-case power
  - Worst sustainable power
- Fact
  - Power is highly dependent on input pattern statistics
  - Input patterns are usually highly correlated and vary with time
- Result
  - Average power vary with time
  - Algorithmic worst-case power rejected for excessive pessimism
Power Management Status

• Continuous push towards deterministic reduction of dynamic and leakage power
  ▪ Dynamic power reduction
    • Multi-voltage
    • Dynamic voltage scaling
    • Clock gating
  ▪ Leakage power reduction
    • Multi-Vt
    • Power gating
    • Back bias
• Create distinctive power consumption “modes” in circuit operation
Power Management vs. Analysis

• Power “signature” analysis at block level
  ▪ Capture deterministic “mode” behavior
  ▪ Additional sensitivity analysis to model other dominant signals
  ▪ Statistical or probabilistic approaches for the rest of signals
  ▪ Can be easily extended to power macro model

• Power “configuration” at chip level
  ▪ Capture architecture impact on power consumption
  ▪ Capture system operation in sequence of configuration switches
Power Management is not Free

- Lower supply voltage lowers noise margin
- Multi-mode control of circuit function worsens gradients of current distribution, leading to Ldi/dt noise
Power Supply Noise Analysis

**Parasitic Extraction**
- P/G RC
- Signal RC
- Package RLC

**Power Analysis**
- Block level power signature analysis
- Chip level power configuration

**Library Characterization**
- Voltage-dependent timing models
- Current waveforms
- Intrinsic parasitics

**RLC**

**SSO**

**Library**

**STA**

**Dynamic Analysis**
- Dynamic voltage drop analysis
- Electromigration analysis
- SSN

**Voltage-drop-dependent Timing Analysis**
Voltage-Dependent Timing Models

\[(\text{Delay}, \text{Slew}_{- \text{out}}) = f (\text{Slew}_{- \text{in}}, C_L, \Delta V_{DD,\text{IN}}, \Delta V_{SS,\text{IN}}, \Delta V_{DD,\text{OUT}}, \Delta V_{SS,\text{OUT}})\]
Power Supply Noise

- Challenges how we characterize library
  - Explosive simulation complexity needs to be dealt with seriously
- Challenges how we analyze power
  - Systematic, hierarchical approach is needed
- Challenges how we analyze timing
  - Consider dynamic voltage drop in STA
- Challenges how we partition the problem
  - SSN needs to be considered in noise analysis
- Challenges tool capacity and speed
  - Is overnight run on a 20M gate design possible?
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A Glance into the Future

- Tuning / Overhauling of existing software infrastructure will continue
- Analysis engines with high accuracy and efficiency will become a must and bigger a challenge
- Catering to all care-about’s in implementation engines is a tough balance act
- Understand analog behavior to continue the path of digital designs
  - Library characterization
  - Delay calculation
  - Dynamic voltage drop effects
A Glance into the Future (cont’d)

• Crosstalk flow needs to be improved
  ▪ Convergence
  ▪ Pessimism removal
  ▪ Closure

• Approach power analysis from architectural view

• Power supply noise will get more mind- and time-share

• Understand limitation of automation
  ▪ Intuitive interface to collect design-specific knowledge avoids over- and under-optimization and excessive runtime