Integration and Interoperability Requirements for IC Design in the Year 2000

John Darringer
IBM Microelectronics

presented in 1998
Agenda

- Technology evolution
- Impact on design and design systems
  - Yesterday
  - Today
  - Tomorrow
- Integration requirements
Yesterday’s Technology

- 260K Gates
- Uniform structure

Static Circuits

4-5 Layers of Interconnect
Coupling Cap = 44% Self Cap

3.3Vdd
Yesterday’s Design System Evolution

- Synthesis considers actual timing impact
- Timing recomputed for changed nodes only
- Significant improvement in timing closure

Incremental Timing Analysis
Today’s Technology

- 3.3M Gates
- Variety of macros
- Some Dynamic Circuits
- 5-6 Layers of Interconnect
  Coupling Cap = 62% Self Cap
Today’s Design System Evolution

- Synthesis and placement consider actual timing change
- Only effected gates placed
- Significant improvement in design closure
Tomorrow’s Technology

>10M Gates
Wide variety of macros

Sensitive Dynamic Circuits

1.5Vdd

>6 Layers of Interconnect
Coupling Cap = 73% Self Cap
Other sources of noise
• Incremental synthesis, placement, and wiring available to solve timing and noise problems
• Necessary for design closure
New Design System Architecture

- Common data model
  - In memory
- Incremental applications
- Modular applications
- Cockpit controls methodology
- Standard interfaces for data and control
  - New standard process required
Tight coupling only for significant methodology benefit
Summary

- Technology continues to advance
- Designer must deal with more issues
  - Area – Power
  - Performance – Noise
  - Time to market – Yield
- Design systems must keep pace
  - New and improved applications
  - Tight integration of key functions
  - Incremental processing
  - Multi-company effort
- New standards are needed
  - Interfaces for tight coupling applications
  - Process for rapid standard development
Interoperability Workshop at DAC

Sunday June 4, 12:00 - 5:00, Fee=$40 - $60

- **Session 1 - Do we need a Standard Data Model API?**
  - What are the Requirements?
    - Terry Blanchard - Mgr. VLSI Technology Center, HP
    - Thomas Daniel - VP ASIC Technology, LSI
    - Sumit Dasgupta - Mgr. Tools and Methodology, Motorola
    - Jennifer Howland - Dir. EDA, IBM
    - Jan-Olof Kismalm - Dir. Microelectronics Coordination, Ericsson
    - Mark McDermott - Dir. Texas Development Center, Intel

- **Session 2 - What is required to achieve a Standard API?**
  - Tbd, Avant!
  - Dinesh Bettadapur - VP Business Development, Monterey
  - Raul Camposano - VP R&D, Synopsys
  - Jim Hogan - President Cadence Design Systems, Japan
  - Joe Hutt - VP R&D, Magma
  - Kent Moffat - Group Mgr. Solutions Partnerships, Mentor Graphics

- **Session 3 - What is the Action Plan for 2000?**
  - Panel Chair Richard Goering - Editor EE Times
Input from IEEE EDP Workshop

- Session 1 - Do we need a Standard Data Model API? What are the Requirements?
- Session 2 - What is required to achieve a Standard API?
- Session 3 - What is the Action Plan for 2000?