FinFETs
State of The Device

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AGENDA

• From Planar to Multi-Gates (FinFET)
• FinFETs Today
• Device Technology – 10nm and Beyond
• Summary and Conclusions
Progression from Planar to Multi-Gates

- Gate coupling to substrate getting weaker with scaling
- Control does not exceed 5nm from surface

**Gate**

\[
\begin{align*}
V_{gs} & \quad C_g & \quad V_{gd} \\
V_{s} & \quad \text{Source} & \quad \text{Channel} & \quad V_{d} & \quad \text{Drain} \\
V_{d} & \quad \text{Vs} & \quad \text{Vd}
\end{align*}
\]

- \( L_g = 25 \text{ nm; } T_{ox,eq} = 12\text{Å} \)
- \( T_{Si} = 10 \text{ nm} \)
- \( T_{Si} = 20 \text{ nm} \)

Leakage Current Density [A/cm²]

\[
I_{off} = 2.1 \text{ nA/μm} \quad I_{off} = 19 \text{ μA/μm}
\]

\( T_{si} < \frac{1}{2} \times L_{fog} \) good channel control
FinFET Design Considerations

- **Fin Width**
  - Determines short channel effects

- **Fin Height**
  - Determines Current
  - Limited by etch technology
  - Also limited by mechanical stability

- **Fin Pitch**
  - Determines layout area
  - Limits S/D implant tilt angle
  - Tradeoff: performance vs. layout efficiency
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Status of FinFET technology today

- 22nm Trigate is in full production
- 16nm / 14 nm proven is silicon (testchips)
  - Production (yield) 1 to 2 years away
- 10nm: No major show-stoppers
  - Major Foundries working on it for over a year
  - Tools are in intermediate stages of development / partner interaction
  - The metrics of accuracy, performance and run time dominates
- The 10 nm device is FinFET
  - Channel and Source/drain engineering is focus
  - Interconnect reaching the limits $\tau = 80\text{ns}$ – significant bottleneck!!
    - Layout and design experience make a HUGE impact
    - IP architecture is critical
Status of FinFET technology today

• Feasibility & Cost are two major factors in determining among Litho alternatives (LELE vs. SADP, etc.)
  – Has Layout Rules, Tools and IP implications)
• On the surface ….. Tools for 10nm are no different than for 14 nm /16nm given the device is more or less the same… but to maintain the triad of Accuracy, Performance, and Runtime,… tools are significantly impacted
• Largest impact on tools will be in
  – Simulation
  – Lithography
  – IP / Routing
  – Extraction
  – Verification (special constructs, fuzzy pattern matching), etc.
Some challenges for 10nm technology

• Simulation:
  – Netlist elements growing 3X-5X compared to 28nm
  – More complex BSIM-CMG model
  – Higher switching speeds -> smaller time-step -> simulation time without tools enhancements is 12X slower than planar.
    – Multi threading + other simulation enhancements brings it back to 2X-3X range
• Lithography: converging on solutions for 10nm
  – Spacer is Poly (SIP) for gate, LELELE (TPT) for M1 and contact, Spacer is Dielectric (SID) for Mx layers. QUAD patterning for 10nm lower interconnect?
  – TPT decomposition likely to be done by designers.
    – Subject of debate
Double Patterning Technology

- Double exposure: a sequence of two separate exposures of the same photo-resist layer using two different photo-masks.

  - Photoresist coating
  - First exposure
  - Second exposure at different locations
  - Development of both exposures in the photoresist
Self-aligned Spacer: Basic Review

- A spacer is a film layer formed on the sidewall of a pre-patterned feature
- There are two spacers for every line, the line density has now double

1. First pattern
2. Deposition of mask material
3. Etching to/from sidewall spacers
4. Removal of first pattern
5. Etching using remaining spacers as mask
6. Removal of spacer, leaving final pattern
Spacer Lithography – Rinse and Repeat

Photo-lithographically defined sacrificial structures

1st Spacers

2nd Spacers

3rd Spacers

$2^n$ lines after $n$ iterations of spacer lithography!

- Many flavors of Spacer Lithography
  - SIP, SADP, SID, etc..
  - Flavor of Spacer has cost, tolerances, design rules, and verification implications
Double Patterning (DPT) Options

Litho-etch-litho-etch (LELE)

- Litho1
- Etch1
- Litho2
- Etch2
- HM Remove

“Stitching” of patterns possible

Self-aligned double patterning (SADP)

- spacer = space (SID)
- Litho
- Etch mandrel
- Spacer
- Fill
- Etch
- Remove
- spacer = line (SIP, SIM)

SADP requires additional trim masks

• Double patterning introduces significant variability in device and interconnect performance:
  • LELE: impacted by CD and overlay of each patterning step
  • Spacer: impacted by CD variation of mandrel, overlay only for trim masks (usually uncritical)
• Choice per layer depending on cost, variability needs
More on SADP – Positive / Negative Tone

**Positive Tone:**
- Large flexibility on feature width and space
- Non-sidewall regions covered by trim mask are exposed
- Exposed material will be etched out to be the feature

**Negative Tone:**
- Sidewall regions define the trench
  - Design inflexibility
- Sidewall + NOT covered by trim is the trench / feature

Notice impact of sidewall / Trim on overlay

Diagrams from Zhang et al, 2013
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Evolution of Transistor Scaling

- L used to be in sync with technology node
- L quickly accelerated then saturated
- Will fall behind

Size, nm

1um 0.7um 0.5um 0.35um 0.25um 180nm 130nm 90nm 65nm 45nm 32nm 22nm 14nm 10nm 7nm 5nm
Device beyond 14nm: scaling to 3.5nm

Transistor Structure for 10nm and 7nm nodes

- **UTBB**
  - Ultra Thin Body & BOX

- **FinFET/Trigate**
  - « Vertical » double gate
  - Undoped or doped channel
  - Multi-Fin
  - Raised S/D

- **Nanowire**
  - Gate-All-Around
  - Undoped channel
  - Multi-wires
  - Raised S/D

Challenges of 10nm and 7nm CMOS Technologies, IEDM Short Course, Dec. 8th 2013

From Frederic Boeuf, IEDM
# Expected Design Rules

<table>
<thead>
<tr>
<th>Foundry node</th>
<th>Gate pitch</th>
<th>L</th>
<th>Spacer</th>
<th>Fin top</th>
<th>Fin bottom</th>
<th>Fin height</th>
<th>Fin pitch</th>
<th>Contact size</th>
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<tr>
<td>16 / 14</td>
<td>90</td>
<td>25</td>
<td>18</td>
<td>5</td>
<td>15</td>
<td>35</td>
<td>48</td>
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<td>11</td>
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<td>16</td>
<td>5</td>
<td>3</td>
<td>2D material</td>
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<td></td>
<td>10</td>
<td>5</td>
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## Technology

<table>
<thead>
<tr>
<th>Technology (foundries)</th>
<th>10nm</th>
<th>7nm</th>
<th>5nm</th>
<th>3.5nm</th>
<th>2.5nm</th>
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<tbody>
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<td><strong>L, nm</strong></td>
<td>20</td>
<td>15</td>
<td>11</td>
<td>7.5</td>
<td>5</td>
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<td><strong>Transistor architecture</strong></td>
<td>FinFET</td>
<td>FinFET</td>
<td>Nano-wire</td>
<td>Nano-wire</td>
<td>2D material</td>
</tr>
<tr>
<td><strong>Materials</strong></td>
<td>Si</td>
<td>Si, SiGe, InGaAs</td>
<td>Si</td>
<td>Si</td>
<td>MoS₂</td>
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<tr>
<td><strong># of atoms in the channel</strong></td>
<td>300 k</td>
<td>100 k</td>
<td>10 k</td>
<td>3 k</td>
<td>300</td>
</tr>
</tbody>
</table>

From Victor Moroz, Synopsys
Beyond FinFETs

Each NW contributes less due to quantum separation.

Current is harvested from ~24 nm out of 30 nm.

Stack of NW has to be ~3x taller than the fin...

14nm node
10nm node
7nm node
5nm node

From Victor Moroz, Synopsys
Beyond Nano-Wires

Stack of 2D channels has to be ~10x taller than the fin...

Aspect ratio: 50:1 !!!

Imaging self-heating!

From Victor Moroz, Synopsys
“Si MOSFET” NW has similar structure to the TFET shown, with n+ source and n+ drain.

Only one TFET material combination with broken gap heterojunction gets close to the Si nano-wire.

And only for the n-type.

Nothing comparable has been found for the p-type so far.

Comparison of drain current for different N-TFET materials and Si MOSFET using atomistic simulations. (Vds=0.3V, Lg=13nm and Ioff=10pA/um target)
Surprisingly, TFET variability is comparable to the MOSFET’s.

For both, variabilities are dominated by the WF due to the bad assumption of metal grains not shrinking between now and 2018.

The MOSFET beats TFET at HP.

They are comparable @SP.

The TFET is better @LP.
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Summary

• 14/16nm on track, and 10nm is under development
• FinFETs are scalable to 7nm node, maybe beyond
• Interconnect challenges tremendous @ 10nm / beyond
• Manufacturability issues abound
• Variability trend is encouraging
• Non-Si channels boost Ion, but suffer BTBT leakage
• Self-heating will get worse over time
• Nano-wires and TFET devices promise scaling to 2.5nm
• TFETs have a promise of sub- 0.4V VDD scaling
• EDA tooling / IP techniques challenges NOT trivial