Evolving BIST Solutions for 3D-ICs

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EDPS 2012
3D IC Test Challenges

Known good die (KGD) requirement

Known good interposer requirement

Partial stack testing

Memory to logic TSV testing

Logic to logic TSV testing

Die test in package
ENSURING
KNOWN GOOD DIE
Stacking Approaches

Wafer-to-wafer (W2W) Bonding

- Works only with homogeneous die
- Very difficult to control individual stack yield

Die-to-wafer (D2W) Bonding

- Necessary for heterogeneous stacked die
- Stack yield controlled with KGD and partial stack testing
**Known Good Die Requirement**

Die Defect Coverage

\[ \text{DC}_D \]

Final Package Yield

\[ \prod \text{DC}_{D_i} \]

... For 10 Die Stack:

<table>
<thead>
<tr>
<th>DC_D</th>
<th>( \prod \text{DC}_{D_i} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>90%</td>
<td>35%</td>
</tr>
<tr>
<td>95%</td>
<td>60%</td>
</tr>
<tr>
<td>99%</td>
<td>90%</td>
</tr>
<tr>
<td>99.9%</td>
<td>99%</td>
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</tbody>
</table>

Still 10 times more wasted packages and test time
Known Good Die Requirement

Need comprehensive wafer test coverage

High coverage of multiple fault models
Stuck-at, TDF, N-Detect, Cell-Aware, ...

Contactless parameter measurement
Jitter, sampling instant, BER, ...

Contactless performance test
Leakage, delay testing, ...

At least basic coverage of common functions
PLLs, ADC/DAC, filters, ...
Contactless Test of Regular IO
IO BIST

- Propagation delay measurement using Bscan
- BIST provides high-speed Bscan control signals
- Delay-difference measurement eliminates signal propagation variations and noise
- Rise and fall delay measurement with resolution adjustable from nanoseconds to picoseconds
Contactless Test of SerDes IO

SerDes BIST

- Accurate picosecond measurements of critical parameters
  - Jitter (Random, Total)
  - Jitter Tolerance
  - Rise/fall time, Slew rate

- RTL-based, vendor independent BIST

- No changes to physical IP under test
TEST ACCESS FOR STACKED DIE
Typical 3D Package Components

- DRAM Die
- Wide I/O TSV Bus
- Multiple SoCs (with DFT)
- TSV Interconnect
- I/O to outside
Test Access Within Stack

- Dedicated TSVs used for test signals between die
  - Can include scan channels

- Control hardware needed to route test data up and down stack

- Standard architecture necessary to support heterogeneous die from multiple vendors.
  - IEEE P1838 under development
TESTING DIE WITHIN 3D STACK
Die Test In-Package

- BIST best suited for re-test of die within stack
  - Very limited data bandwidth required
  - Very limited test data storage on tester required
  - Dies can be tested in parallel to minimize test time
BIST for Stacked Memory Test

- External Memory BIST added to logic die
  - Provides full-speed testing of memory die and bus
- Post-silicon programmability supports changes in memory die
BIST for Stacked Memory Test

- All BIST transactions performed through functional PHY interface
  - Interface handles all signal synchronization
  - Interface also handles mux/demuxing for DDRs

- BIST supports all forms of DRAM access
  - Bursting, Refresh, etc

- BIST highly programmable
  - Address range and read/write operations for supporting different memories
  - Algorithms for different quality and test cost needs
    E.g. Interconnect only coverage

- Supports bussed memories
Memory Built-In Self-Repair

- Repair process performed completely on-chip
- Repair info stored in on-chip programmable fuse array
- Repair can be performed at multiple stages
  - Wafer test
  - Final test
  - Post-stack test
- Critical for achieving yield
Built-In Self-Repair of TSVs

- Similar in concept to mature memory BISR approach
  - Connectivity enhanced with redundant TSVs
  - TSVs tested and diagnosed
  - Repair information is stored in e-fuse box
  - Upon power up the connectivity is configured by Fuse Controller
BIST Support of Corel-Level Redundancy

- Parallel processing key to growing integration levels
- Possible stack yield management through redundant cores
  - Initial yield improvement or graceful degradation
- BIST provides fully autonomous availability check
Summary

- Plenty of 3D Test related challenges
  - Test access, quality and yield improvement
- BIST solutions will play a key role in 3D test
- Existing commercial BIST solutions directly applicable to 3D
- Improvements and new BIST capabilities for 3D under development