EDA Needs for FPGA

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Outline

- Overview
- Desired EDA flow
- Altera’s Needs
- Future Directions
Times Have Changed

1990s
- Glue Logic
- Heterogeneous Capabilities
  - Flex 6000 30µ process
  - Stratix I 130nm process

2010s
- High Integration/Bandwidth
  - Stratix IV 40nm process
- Hardened Subsystems
  - Stratix V 28nm process
- Cortex-A9 MPCore
  - SoC FPGA 28nm process
Silicon Convergence

Software Programmability

Hardware/Software Programmability

Limited or No Software Programmability

MPU  DSP  FPGA  ASSP  ASIC

FPGA Platforms Ideally Positioned for Convergence
Silicon Convergence Laying Foundation for 3D

- Bandwidth expansion
  - High-bandwidth chip-to-chip interface (JEDEC wide IO interface)
  - Optical interconnect

- Additional processing capabilities
  - Memory enhancement

- Product feature set expansion and time-to-market
  - Derivative products

- Energy efficiency

- Integration
  - Fewer components
Altera’s 3D Silicon Vision

- Customer & application driven heterogeneous system integration in package
  - Mix and match silicon IP
  - Integrated design flow
  - Integrated system test methodology
- Maximum system performance
- Minimum system power
- Smallest form factor
- Reduced system cost
Altera’s Product Development Strategy

Product Definition

Manufacturing & Supply Chain

Architecture & Design Infrastructure

Ecosystem & Standards

Design Tools Influence
- Efficiency (productivity & TTM)
- Quality
- Business models
- End user’s experience
Altera and TSMC Jointly Develop World's First Heterogeneous 3D IC Test Vehicle Using CoWoS™ Process

Altera Leveraging TSMC’s CoWoS Manufacturing and Assembly Process for Development of Next-Generation 3D Devices

San Jose, Calif., and Hsinchu, Taiwan, March 22, 2012—Altera Corporation (Nasdaq: ALTR) and TSMC (TWSE: 2330, NYSE: TSM) today announced the joint development of the world’s first heterogeneous 3D IC test vehicle using TSMC’s Chip-on-Wafer-on-Substrate (CoWoS) integration process. Heterogeneous

CoWoS: Chip on Wafer on Substrate
Desired EDA Flow for 3D Integration

Planning & Pathfinding
- 2D monolithic IO/bump/RDL
- 2.5D/3D die stack planning
- RTL resource partitioning for tiers

Physical Design Implementation
- 2D monolithic IO/bump/RDL
- 2.5D/3D die stack configuration
- TSV/u-bump/C4 bump/RDL
- RTL synthesis, P&R, & verification

Performance Validation
- SI/PI/IR/EM
- Thermal & Timing
- Die and package routing density

Verification
- LVS
- DRC

Tape-out
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Tape-out

Collaterals
- TSV/u-bump model & library
- MFG rules for die stack planning, yield model, and cost estimates
- Material properties
- Tech file and PDK
- Manufacturing design rules
- Auto RDL (IO-to-bump and chip-to-chip)
- Calibrated models for electrical, thermal, and thermo-mechanical analysis
- System level-timing model
- Infrastructure to handle multiple GDS handling (2-3+)
- Different process nodes with die shrink
- Auto TSV/u-bump layer mapping
- Chip-to-chip mfg rule check
## EDA Gaps

<table>
<thead>
<tr>
<th>Focus Areas</th>
<th>Path finding</th>
<th>Tier Design &amp; Verification</th>
<th>Die Stack Verification and Perf. Validation</th>
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<tbody>
<tr>
<td>Design Partitioning &amp; Chip-Package Co-Design</td>
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<td>Abstract Views</td>
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<td>Physical, Functional, and Timing Verification</td>
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<td>SI/PI Analysis</td>
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<td>Thermal Analysis</td>
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<td>Yellow</td>
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<tr>
<td>Thermo-mechanical Assessment</td>
<td>Yellow</td>
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<td>Others: data exchange, scalability of database, etc.</td>
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<td>Red</td>
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- **Green**: Flow exists
- **Yellow**: Existing flows can be adapted
- **Red**: Needs EDA support
Pathfinding for Early Assessment

- Stacking configurations and chip-package interaction
  - System requirements => partitioning => tier requirements
  - Thermal and thermo-mechanical analysis based on macro models (effective material properties)

- 3D product specification
  - Architectural, functional, electrical, and test
  - Structural (intra-tier, inter-tier, and TSV/u-bump/bump planning)
Pathfinding for Early Assessment (Gaps)

- Existing RTL-to-GDS and Die/Packetage co-design flows are too cumbersome for quick and cross-functional what if analysis
Pathfinding for Early Assessment (Gaps)

- Existing RTL-to-GDS and Die/Package co-design flows are too cumbersome for quick and cross-functional what if analysis
Physical Design Implementation: Tier Planning

- Floor planning
  - Application mapping
  - Dependencies among application specific hard/soft IPs
  - Use model

- TSV, u-bump, and bump planning
  - Intra- and inter-tier connectivity and performance optimization

- Manufacturing and keep-out rules
Physical Design Implementation (Gaps)

- DRC and LVS of individual tier and tier-to-tier interface (divide and conquer strategy)
  - Custom ad hoc methods invented on the fly vs. standard approach for tier-to-tier DRC/LVS
  - Challenges with multi-vendor or mixed-technology integration

- Visualization for debugging and FA
  - Navigating through different databases

- Managing database size and process shrinks
System Level Performance Validation (Gaps)

- Multi die power sign off is challenging due to large database sizes
  - Basic EDA infrastructure exists for abstracting die’s (e.g. CPM), but these are yet to evolve completely in mainstream flows

- Multi die STA is extremely challenging in 3D IC while complexity is manageable in 2.5D IC

- Multi die connectivity management for system level LVS
  - More convergence between IC schematics tools and SIP tools desired to bridge the gap between chip and system
System Level Performance Validation (Gaps)

- Chip-to-chip timing closure: SPICE & STA
- Signal integrity analysis
  - TSV and chip-to-chip interconnect coupling and cross talk
  - High speed chip-to-chip signaling loss

- PDN and Thermal
Future Trends
Extension of Existing Standards and Known Good Methods for Die-Stacking

**Standard Cells**
- Physical, Logical, & Abstract Views
- Timing, Power, & Parasitic
- GDSII, RTL, LEF, LIB, & TLF

**IP**
- IP-XACT/IEEE Std 1685
  - Hardware information
  - Software views, file lists, protocol standardization
  - Describes the interface to IPs, but not functionality
- In many cases
  - tool centric
  - determined by customers

**Stacked IC**
- Design & verification of each tier & overall system
- Tier-to-tier interface
  - Electrical
  - Functional
  - Physical
  - Timing
- Data format
  - Verification
  - Thermal
  - Thermo-mechanical
  - Chip-package design
Convergence in Manufacturing

- Die stacking approaches and design rules are converging
  - Flavors integration
  - TSV and micro-bump size and pitch
  - Wafer thickness, BEOL stack for 2.5D, RDL for 2.5D/3D, etc.
  - Standards: http://wiki.sematech.org/3D-Standards

- Enables economies of scale and faster adoption
  - EDA industry needs to be vocal
Die Stacking is an Enabler for System-Level Integration

- FPGAs have been gradually incorporating system-level functions
- Die stacking provides unique business opportunities
  - Moving up in value chain
  - Time-to-market and product differentiations
- EDA tools need to evolve to support higher-level system integration enabled by die-stacking
Thank You
The Dilemma: Flexibility vs. Efficiency

Reconfigurable Co-processors

Alterna at a Glance

- Founded in Silicon Valley, California in 1983
- Industry’s first reprogrammable logic semiconductors
- $1.95 billion in 2010 sales
- 2,600 employees
- Leading supplier of FPGAs, ASICs and CPLDs