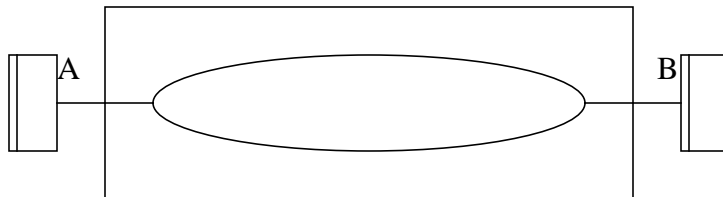


7 ns - (target clock arrival - source clock arrival) - clock uncertainty - register setup

CASE 1



CASE 2

