Advanced EDA Benchmark Program: Status Report

Supported by IEEE Circuits and Systems Society
Managed by Semiconductor Research Corporation

April 19, 1999
Objectives

◆ Acquire datasets for several “large” chip designs
  – From industry.
  – State of the art, or close to it.
  – Remove proprietary information.
  – Make datasets widely available to researchers, EDA companies, EDA users.
◆ Establish a permanent repository for Advanced Benchmark Datasets
◆ Develop a community of interest to sustain the effort.
Program Participation

◆ **Funding**: IEEE Circuits and Systems Society
◆ **Program Management**: Semiconductor Research Corporation.
◆ **Industry**: IBM, Sun Microsystems, LSI Logic, MITRE Corporation, Mentor Graphics, SEMATECH
◆ **All are welcome**! Web site and majordomo:
  – Contact: benchmrk-owner@eda.org
  – Information: http://www.eda.org/benchmrk
  – Email discussion: benchmrk@eda.org
First Project: Vertical Benchmarks

- Multiple representations
- Complete standard design flow

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representation
Behavior → HL Synthesis
Structure → Logic Synthesis
Gate → Physical Design
Geom/Trans. → Perf. Analysis
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Design Flow
A Vertical Benchmark: CMUDSP

http://www.ece.cmu.edu/~lowpower/benchmarks.html

- Based on commercial DSP architecture
- 4x larger than any of listed benchmarks
- Fabricated in 0.5µm (30MHz)
- Diversity:
  - Memories
  - Control
  - Data path
MITRE Design: 2048-Tap Reconfigurable FIR Filter

- Hewlett-Packard 0.5μ CMOS low-power
- 1½ Million Transistors, 64Kbits RAM
- 6 billion operations/sec
- Dual coefficient register banks: suitable for adaptive filter applications
- Saturating arithmetic operations (maximizes dynamic range)
- Full-scan sequential logic (improves testability and reliability)
- Dual-mode interface: configured by ext. ROM (no glue-logic) or by µprocessor
- Throughput: 65M samples/sec
- 352-pin TBGA package
Program Status

😊 IEEE CAS has approved the first project:
  - Funding start anticipated before end of April 1999
😊 This is a one-quarter delay from previous plan.

◆ Project Plan:
  - **Collaboration** between CMU and MITRE Corp.
  - **Principal Investigator**: Herman Schmit (CMU)
  - **June**: Behavioral description of CMUDSP complete; Silicon Ensemble flow complete
  - **July**: MITRE design moved to CMU
  - **August**: MITRE design reimplemented in CMU flow
  - **October**: Test methodology for CMUDSP
  - **December**: Release both designs
New: CMU Cell Library

Because of potential problems with Duet library, Prof. Herman Schmit and students are developing a public domain cell library:

- HP 0.35 $\mu$m rules (not MOSIS with $\lambda = 0.2$)
- 116 cells: 96 gates, 16 flops (with and without scan), 4 latches
- 10 pad cells (10 $\Omega$ and 50 $\Omega$, 3.3 v, no bidirectionals or 5 v tolerant IOs)
- Intrinsic inverter speed: 80 ps
CMU Cell Library Status

◆ Built 4,000-gate designs with the library
◆ Will have fabbed chips at release
◆ Beta release: early summer
◆ Planned release: Fall 1999

◆ Contact:
  – Prof. Herman Schmit, Carnegie-Mellon U
  – (412)268-6470
  – herman@ece.cmu.edu
Other Benchmark Activity

◆ Collaborative Benchmarking Laboratory (Franc Brglez)

http://www.cbl.ncsu.edu

◆ ITC Benchmarks (Scott Davidson)


◆ Manchester STEED Project (Hilary Kahn)

http://mint.cs.man.ac.uk/projects/steed/
Questions? Answers?