

# Accellera Verilog++ Assertion Extension Requirements Proposal

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## Abstract

*This paper is intended as a strawman requirements proposal for assertion extensions to IEEE-1364 Verilog.*

## 1. Introduction

This document is intended to form a strawman proposal for the IEEE-1364 Verilog assertion extensions. While establishing a set of requirements for the Verilog assertion extensions, the committee should consider the following goals:

- *Expressiveness*: The assertion extension should be expressive enough to cover most implementation properties likely to be used by the design engineer.
- *Usability*: The assertion extension must be easy to understand and use by the design engineer.
- *Formalism*: The assertion language must have rigorous formal semantics to ensure correct compilation.

**NOTE:** *This document should **not** be considered the official Accellera Verilog++ Assertion Extension Requirements Document. The intent of this document is to propose a set of requirements that should be considered when creating the final Assertion Requirements Document. In addition, this document does not set any requirements on assertion implementation or syntax.*

**Assertion Extension Justification:** The question arises whether assertion extensions are necessary. After all, many Hardware Verification Languages (HVLs) provide powerful language features that can be used to describe correct temporal behavior. These HVLs can be used for data generation and results analysis thru temporal specification. In addition, the Accellera Formal Verification committee is actively defining a property specification language that can be leveraged by multiple verification processes. Therefore, some will say either HVLs or formal Property Languages *should* be able to provide all the power necessary to express assertions within the design. However, a variety of stakeholders in the design and verification flow necessitates a variety of approaches to specifying design properties.

The reality of the contemporary design and verification flow requires a broader look at the issues, and an understanding of the goals of the various stakeholders. The value white-box testing (through assertions) provides over a black-box testing approach has been validated by numerous sources. [Kantrowitz and Noack DAC 1996] [Taylor et. al. DAC 1998] [Bening and Foster Kluwer 2000] [Switzer et al. HDLCon 2000] [Foster and Coelho HDLCon 2001]. And, white-box testing can be performed with assertions, HVLs, or formal property languages. However, experience shows that verification engineers, whose goal is design validation, prefer an HVL approach to specifying properties of the design. On the other hand, the design engineers' focus is on implementation using hardware description languages (HDLs).

In addition to the dichotomy of goals, this issue also encompasses the areas of expertise of the various stakeholders. Quite often, the verification engineer lacks sufficient in-depth knowledge of design implementation details to provide effective white-box assertion coverage. On the other hand, during the course of RTL development, the design engineer makes low-level assumptions about the design's environment as well as other implementation assumptions. Experience has shown that if design assumptions or concerns are not captured during the process of RTL implementation, then many

lower-level implementation properties are lost (that is, they will not be verified). For example, the *verification engineer* might wish to verify that a PCI bus controller exhibits correct behavior. This can be accomplished by using an HVL to generate correct bus functional stimulus and validate correct bus functional results. The verification engineer, however, would not validate specific implementation properties. Continuing with this example, assume that the PCI controller contains multiple embedded state machines. The *design engineer's* decision to implement a particular state machine as a one-hot versus some other type encoding is irrelevant to the verification engineer--provided that the PCI controller exhibits correct bus functional behavior. Yet, capturing properties of the implementation (for example, one-hot) during the design process provides better white-box coverage.

Ultimately, the most effective overall approach for capturing *implementation* properties is to include assertions as part of the HDL during RTL development. Assertions directly encoded within the HDL, versus maintained separately through HVLs or property languages, simplify the integration of reused blocks (that is, design reuse). Experience has shown that difficult forms of assertion specification limit the number of assertion capture during the implementation process--thus poorer quality of white-box coverage. Furthermore, revisiting the HDL after the implementation phase to add in assertions also results in a poorer quality of white-box coverage.

Hence, although there is some overlap in HDL assertion specification, versus HVL and Property Language specification, the end user of the particular form of specification is different. Thus, convenience of HDL assertion specification must be a consideration. This paper is intended to form a strawman proposal for assertion specification targeting the design engineer during Verilog implementation.

## 2. Definitions

### 2.1 Event

In this strawman proposal we define an *event* as a Verilog expression, which evaluates to a TRUE value at some point in time  $t$  during the course of verification. For example, if the expression  $(c\_ready == 1)$  evaluates TRUE at time  $t$ , then an *event* has occurred at time  $t$  in the verification environment.

### 2.2 Assertion

An *assertion* is a claim we make about an event or a sequence of events associated with the Verilog model. The assertion claims may be classified as either an *invariant* or a *liveness* property.

#### 2.2.1 Invariant

An invariant assertion is a static event that must be valid for all time. There is no time relationship of events associated with an Invariant.

#### 2.2.2 Liveness

A liveness assertion possesses *temporal* behavior. In other words, there is a time relationship of events associated with it, whose correct sequence must be valid. For example, a temporal assertion can be viewed as an event-triggered window, bounding a specific property, i.e., an event.

### 2.3 Assertion Expression

The assertion expression is an event represented by a Verilog expression.

### 2.4 Assertion Firing

The term firing in this proposal constitutes the condition when an assertion is violated,

## 3. VHDL Assertions

Details on the VHDL assertion statement are included in this proposal to provide the reader with an example on how other HDLs have implemented a simple assertion mechanism.

VHDL provides a language construct for specifying a *static invariant* assertion in procedural code. For example:

```
[label] assert event
           [report message]
           [severity level]
```

The VHDL assertion statement checks that a specified condition (i.e., event) is true in a procedural fashion and reports an error if it is not.

The optional report clause specifies a message string to be included in error messages generated by the assertion. In the absence of a report clause for a given assertion, the string "Assertion violation" is the default value for the message string. The optional severity clause specifies a severity level associated with the assertion. In the absence of a severity clause for a given assertion, the default value of the severity level is ERROR.

Evaluation of an assertion statement consists of evaluation of the Boolean expression specifying the condition. If the expression results in the value FALSE, then an *assertion violation* is said to occur. When an assertion violation occurs, the report and severity clause expressions of the corresponding assertion, if preset, are evaluated. The specified message string and severity level (or corresponding default values, if not specified) are then used to construct an error message. The error message consists of at least:

An indication that this message is from an assertion

The value of the severity level

The value of the message string

The name of the design unit containing the assertion.

To express *temporal* assertion or *liveness* properties requires constructing finite state machines to trap the temporal behavior within the VHDL code. The action performed due to a given severity level is determined by the tool.

## 4 Assertion Language Requirements

### 4.1 Syntax Language Features

#### 4.1.1 Assertion Identifier

*The Verilog Assertion Extension should have a unique identifier associated with it.*

For example, if a primitive approach is adopted as the assertion specification mechanism (similar to existing gate primitives in Verilog), then an instance name similar to the gate level primitives could be used for identification. If an attribute approach is adopted as the assertion specification mechanism, a label identifier could be embedded for identification.

#### 4.1.2 Assertion Reset

*The Verilog Assertion Extension should have a mechanism for disabling the assertion.* This reset mechanism will disable the assertions from firing during verification and clears all state maintained by the assertion checker.

#### 4.1.3 Assertion Sampling Clock

*The Verilog Assertion Extension should have a mechanism for defining an optional sampling clock, whose [rising/falling] edge defines the appropriate time to evaluate the assertion expression.*

#### 4.1.4 Assertion Expressions

*The Verilog Assertion Extension should support the entire synthesizable subset of Verilog expressions when representing an assertion expression--including hierarchical references vfv.3@zier. (NOTE: If not, we should explicitly state what is not supported.)*

#### 4.1.5 Assertion Severity Level

*The Verilog Assertion Extension should provide a mechanism for defining the assertion violation severity level.*

The assertion committee might want to define various severity levels (e.g., ERROR, WARNING, NOTE, etc.)

#### 4.1.6 Assertion Violation Action

*The Verilog Assertion Extension should enable the user to define an optional action associated with an assertion violation in simulation.*

For example, *\$finish* called when an assertion fires. Optionally, a user defined *\$PLI* call could be invoked upon an assertion firing. Possibly the user could specify the action as an option to the assertion construct? For example:

```
assert_type -id name -ck my_clock -rst rst_n -severity 0 -expr (a & b | c) -action $my_pli_call();
```

Again, I'm not promoting the syntax listed above. I'm just trying to emphasize that whatever assertion syntax we develop, it is desirable to associate either a *\$finish* or *PLI* call or action with a violation.

#### 4.1.7 Concurrent and Procedural Assertions

*The Verilog Assertion Extension should support both concurrent and procedural assertions.*

A *concurrent assertion's* simulation semantics would be analogous to an instantiated primitive or instantiated module. In other words, the assertion would continuously monitor the *assertion expression* at every edge of a *sampling clock* as long as an assertion reset is inactive.

A *procedural assertion's* is only activated when the particular line of code is visited in a procedural fashion (i.e., the assertion expression is not continuously monitored). If procedural assertions are added as part of the language (and I think they should be seriously studied by the committee as a method of assertion specification), then a clear simulation semantics need to be defined. For example, we would need to define how the simulator would eliminate false firings due to simulation micro-time event execution. One possibility would be to associate (as an option) a sampling clock with a procedural assertion--then if a procedural assertion is activated a call back occurs on the sampling clock to see if the assertion is still invalid.

Formal engines would obviously need to consider the nesting of case and if statements as part of the assertion expression. Experience has shown that user's like procedural assertions (from my own experience at HP). Experience has also shown that user shoot themselves in the foot using procedural assertions due to over constraining the assertion expression by nesting in *if* and *case* statements (i.e., they miss real bugs that would have been caught concurrently).

#### 4.1.8 Event Rise or Fall Detection

*The Verilog Assertion Extension should provide a convenient mechanism for specifying rising or falling events.*

For example, some kind of mechanism such as `-rise(expr)`, which is analogous to something like

```
always @(posedge ck)
    last_expr <= expr;
assign rise = (!last_expr & expr);
```

This feature has been requested by many designers to simplify coding assertion expressions. For example, currently designers detect the rising event as above and then use it in an assertion something like:

```
assert_always test (ck, rst_n, rise ? test_expr : 1'b1);
```

This mechanism would be useful for temporal checks--such as validating the occurrence of multiple events. However, careful thought would be required to introducing any new edge detection mechanism into the language. Could we leverage what already exist?

#### 4.1.9 Setting A Verilog Variable Upon Assertion Violation

*The Verilog Assertion Extension should provide a convenient mechanism for setting a Verilog variable upon assertion violation.*

NOTE: I do not personally favor this requirement since it potentially opens a can of worms. However, I think the committee should at least consider this requirement. This feature would enable the user to buildup very sophisticated assertions using the existing set of lower level assertions. A lot of this would depend on language implementation. For example, this could be easily done with an assertion primitive approach--yet problematic using an assertion attribute approach.

#### 4.1.10 Options or Flags

*The Verilog Assertion Extension should provide a convenient mechanism for enabling tools specific options, such as defining an assertion as a constraint to a formal tool.*

NOTE: This might not be a necessary requirement. The new Verilog 2001 attribute construct might provide sufficient functionality to fulfill this requirement.

### 4.2 Language Constructs and Semantic Features--Classes of Assertions

At a minimum, the Assertion committee should consider two simple construct extensions to the Verilog language. The extensions would consist of (a) a *procedural assertion statement*, and (b) a simple *concurrent assertion statement*.

(a) The simple procedural assertion, as discussed in section 4.1.7, would be analogous to the VHDL assertion construct, with the extension of associating a sampling clock for callback validation.

```
if (q_address > `MAX_QUEUE) begin
    assert @(posedge ck) // <= Only for example, not promoting syntax
    : // Need some mechanism to associate a clock with assertion
```

(b) The simple concurrent assertion, which could be implemented similar to the existing Verilog gate primitive, would follow the semantics of the simple OVL checker. In other words, the concurrent assertion would validate that an assertion expression evaluates to TRUE on every raising edge of a sampling clock.

```
// assertion primitive
assertion .q_overflow (ck, reset_n, (q_address > `MAX_QUEUE), . . . );
```

With these two simple assertions constructs, assertions that are more complicated can be constructed, via libraries similar to the OVL or vendor proprietary languages. In other words, all proprietary languages could be synthesized into a set of FSMs and the two basic assertion constructs. (A RISC approach to building an assertion language). This allows the maximum flexibility in assertion extensions.

Alternatively, the Assertion committee could identify a minimum set of recommended assertion *types* and their semantic meaning. For example, the list could be separated into *invariance* and *temporal* assertions. The list should be derived from the user community experience on common classes of assertion that the designer wished to specify (e.g., HP, etc.). The committee should leverage the assertion experience from other assertion user to derive a comprehensive set (e.g., customers of *Verplex*, *0-In*, *Reallntent*, etc.). Then, an extensive set of assertion constructs could be added to the language. (A CISC approach to creating an assertion language). The advantage to this approach is that it would simplify the designers efforts in assertion specification. The committee should consider both the RISC and CISC approaches.

The following sections identify classes of assertions which have been found useful by HDL engineers with the HP design community.

### 4.2.1 Invariance Assertions

assert always	Verilog assertion expression evaluates always TRUE on the raising edge of a sampling clock.	AG(expr)
assert implication	Verilog assertion expression is checked for implication	AG(X -> Y) Where X and Y are assertion expressions.
assert one hot	Verilog assertion expression is checked for one hot encoding. An option could be provided to permit all zero(one) or one_hot encoding.	AG((n & (n - 1)) == 0) Where n is the assertion expression
assert one cold	Verilog assertion expression is checked for one cold encoding. An option could be provided to permit all one(zero) or one colde encoding	AG((n & (n - 1)) == 0) Where n is the bitwise complement (~) of the assertion expression
assert parity	Verilog assertion expression is checked for even or odd parity	AG(^expr==PARITY) Where PARITY is either 0 or 1, and the expr is an assertion expression.
assert proposition	NOTE: This is similar to assert always -- except there is no sampling clock associated with it. This could be included as a sub-set requirement for assert always.	AG(expr)
assert no overflow	Ensure proper enqueueing and dequeuing behavior based on size of queue--where enqueue and dequeue are represented as assertion expressions. (count enques and dequeues and validate range ).	
assert no underflow	Ensure proper enqueueing and dequeuing behavior based on size of queue--where enqueue and dequeue are represented as assertion expressions. (count enques and dequeues and validate range ).	

### 4.2.2 Temporal Assertions

assert delta	Verilog assertion expression changes values within a specified DELTA range	AG((expr=X) -> AX(expr=X    expr=X+/DELTA))
assert next	Equivalent to the temporal logic AX <sup>n</sup> operator: Given that proposition P1 is true in state s, the proposition P2 will be true at the n-th reachable states from x.	Equivalent to the AX operator.
assert event window change	Ensure that a Verilog expression changes values within an event bounded window.	
assert time window change	Ensure that a Verilog expression changes values with n number of clocks (could be combined with assert window change).	
assert event window unchange	Ensure that a Verilog expression does not change values within an event bounded window.	

assert time window change	Ensure that a Verilog expression does not change values within a time bounded window.	
assert cycles	Ensure that a Verilog expression remains TRUE for a minimum/maximum number of sampling clocks.	
assert frame	Ensure that proper number of cycles between two assertion expression (e.g., B will occur within MIN/MAX cycles after A).	
assert transition	Ensure that a Verilog bit vector (e.g., state) transcends to a legal set of values. Can be used to specify legal state transitions.	
Assert no transition	Ensure that a Verilog bit vector (e.g., state) will not transcends to a specified set of values. Can be used to specify illegal state transitions.	