VHDL in Spain

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Abstract

In this paper a description of the evolution of the usage of VHDL in Spain is provided. Current research and development activities using VHDL at the main companies, Universities and research centers are described. When possible, references have been included in order to facilitate the interested reader access to more detailed information.

1. Introduction

Although VERILOG is still a widely used language, the usage of VHDL in Spain has grown dramatically during the last five years like in other European countries. There are several reasons for this. The first of them arises from the fact that in Spain, RT-logic synthesis and simulation technology developed during the early 90's when almost all of the commercial tools supported VHDL. A second reason is that VHDL has been imposed in many cases externally. On the other hand, many Spanish electronic companies are local branches of a multinational company. On the other, European organizations have played a similar role. This is the case of the European Space Agency which defined VHDL as the hardware description language to be used in any project and, indirectly, the European Commission, which through programs like JESSI, ESPRIT, BRITE, etc., promotes industrial cooperation in research and development projects in which VHDL is usually defined as the common hardware description language. It is worth mentioning the role played by the GAME project. This is an ESPRIT special action for microelectronics in Spain started in 1990 and due to finish in 1996. GAME has provided a very important way to promote ASIC and FPGA design in small and medium enterprises which would not have had access to those technologies otherwise. Although during the first phase the usage of HDLs was very low, during the second phase, started in 1992, the usage of both VHDL and VERILOG has been commonplace. One of the most relevant GAME projects in this area is PRENDA in which a top-down, HDL-based design methodology is proposed focused on facilitating ASIC and FPGA design in small and medium-size companies. A third reason is the growth of VHDL in Universities. Currently, most of the curricula related with electronic design include VHDL at the graduate or post-graduate levels. EUROCHIP, the ESPRIT project supporting VLSI training has provided Universities with inexpensive access to CAD tools.

A good measure of the increased interest in Spain in VHDL is the number of members of the Spanish VHDL Users' Group. Following similar initiatives in other countries in order to put VHDL users in contact, the Spanish VHDL Users' Group was set up in Santander in November 1991. The group started with 15 members. Currently there are 103 members from 30 university departments, 54 members from 23 industrial R&D departments and 10 members from 5 research institutes of Spain, Portugal and South America from a total of 323 VHDL users. The main objectives of the group are to bring together persons and institutions interested in VHDL, to facilitate contact with similar groups in Europe and the USA, to share information and to exchange experiences, to organise courses and seminars of interest to members, to study the joint purchase of tools, to facilitate the distribution in Spain of national and international activities, workshops and conferences on VHDL and
to participate in the standardisation process. The Group is partially supported by a Special Action funded by CICYT, the Spanish research foundation.

The paper is structured as follows. In Section 2, a description of current activities and projects using VHDL at the main companies in Spain is presented. Section 3 describes the usage of VHDL at the University. Finally, activities at the University of Cantabria are presented. Our contribution to the international standardization effort is stressed.

2. Industrial usage of VHDL

There are three the main sectors of the electronics industry in Spain, telecommunication, space and defense. ALCATEL constitutes the most important Spanish electronic company with a large activity in ASIC and system design for telecommunication applications. In all the hardware specification, system simulation and ASIC description, simulation and synthesis tasks, VHDL is used. This has meant that in the ASIC Design Group, the lead time has been reduced by 28% and the designer productivity (gates/person*week) increased by 112% while increasing the circuit complexity by 37%. System specification and gate-level fault simulation and sign-off represent the current bottlenecks in the whole design process.

For ALCATEL Wireless Access, VHDL is at the core of the whole system design methodology. Typically, the design process starts with the definition of the algorithm that is to be used to solve a given problem. As several solutions are usually considered, the designer describes them all in behavioral-level VHDL, and writes a suitable test bench also in VHDL to simulate their functionality and evaluate their performance. Once he/she is satisfied with the capabilities of a couple of mathematical algorithms, the engineer starts working towards their implementation; to do so, he/she refines their high-level descriptions to include several details such as the width of the busses, the precision required for every calculation, etc.; of course, these new architectures are easily simulated with the available test bench. In this step, one algorithm is finally selected, and all the details relevant for its performance are clearly defined [FFR93]. Sometimes, DSPs or microprocessors are used to implement a design; if this is the case, the VHDL files describing its behavior are added to the documentation of the project. If an ASIC or an FPGA is to be used, however, VHDL is also used to describe the device at RT-level, so that it can be synthesized automatically.

TELEFONICA represents the public company in the telecommunication sector. Electronic system design is performed in TELEFONICA I+D (TI+D). In 1990 they started looking for a new ASIC design environment able to handle different foundries with minimum changes and, at the same time, providing the tools required to design complex ASICs with short cycle time and good quality. It was obvious that such a system should be based on HDL and RT-logic synthesis. Both VERILOG and VHDL were considered. Although VHDL could support more complex descriptions and data types, VERILOG was finally selected because a unified design flow from high-level descriptions down to gate level was possible and foundry support both for ASICs and FPGAs was excellent. In the case of VHDL, the situation was quite different, few foundries provided libraries for VHDL simulation and backannotating layout delays was more difficult. The design system has now been in place for quite some time and has proven to work as expected. A number of quite complex ASICs for ATM communication at high frequencies have been developed with very good results [Pla95]. VERILOG represents a good compromise being easy to learn and use and, at the same time, being powerful and fast enough to perform statistical analysis of the algorithms. While in some projects done in cooperation with other companies VHDL is being used, VERILOG is still their mainstream system.

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Within the space industry, ALCATEL ESPACIO also makes intensive usage of VHDL. It represents their standard for describing all digital designs not only for the components themselves, but also for the entire PCB. This is useful for documenting the different components, simulating them and simulating and verifying the whole system. VHDL is used following a strict methodology defined internally that completely fulfills the procedures defined by the European Space Agency (ESA) and which allows the development of both payload equipment (demultiplexers, demodulators, switches, modulators, BFN, etc.) and platform equipment (RTU, PIU, DBU, CDPU, etc.) with a substantial reduction in design time. Other companies in the space sector like INSEL ESPACIO, CRISA and TECNOLOGICA are also using VHDL throughout the design process.

Although the defense sector has decreased its activity during the last years, companies like ENOSA and INDRA still represent a significant part of the whole electronic market. They also design electronic systems for air traffic control applications.

AT&T-Microelectronics in Spain provides both design and fabrication services. They support both VERILOG and VHDL as hardware description languages for the development of ASICs with any of their currently available CMOS technologies: 0.9 μm, 0.6 μm, 0.5 μm and 0.35 μm for both 5 and 3 volts, as well as for its FPGA ORCA Family. On the ASIC library all their macrocells are provided with HDL models (VERILOG and/or VHDL). AT&T Microelectronics development engineers work very closely with 3rd Party Software companies in order to offer their customers support for the latest version of the software. HDL simulators currently (1Q96) supported by AT&T Microelectronics are VSS from Synopsys, QuickVHDL and MTI from Mentor Graphics, Vantage-Optium and Voyager from lKOS supporting VITAL 2.21 compliant timing models and SDF Backannotation. The 3rd Party Synthesis tools supported for VERILOG and VHDL are Design Compiler from Synopsys, Autologic from Mentor Graphics and Express from Exemplar (FPGAs Only).

SIDSA is another design center in Spain using different synthesis and simulation tools. They also represent several CAD vendors and foundries in Spain. Although they use VERILOG in the majority of designs, their experience with VHDL has been decisive in the development of the FICOMP ASIC in the frame of the ESPRIT 6526 project. Now, they are applying the same VHDL-based design methodology to other circuits. The main advantages provided by VHDL have been the following:

1) Design flow support. They have implemented the full design cycle in VHDL. The specification was fixed in VHDL without ambiguities. Synthesis and simulation were done in VHDL improving the speed of the design cycle. The main advantage of VHDL at that step was the possibility of using complex structures in both cases. Although fault simulation and backannotated logic simulation were done in VERILOG, all the input stimuli were obtained from the VHDL simulation.

2) Work in parallel. At the same time they were developing the VHDL ASIC model, the other companies in the consortium were using the model in order to generate the corresponding software. In this way, the software development began one year before the piece was available. Also, this early simulation permitted the establishment of feedback in the refinement of the ASIC model, correcting some undesirable behavior.

3) VHDL as an interchange format. In a consortium composed by CEGELEC (F), EDF (F), MARCONI (I), SOFTING (G) and SIDSA (S), VHDL was used as the common language to communicate the different proposals, models, simulations and specifications among the different companies without ambiguities.

4) Documentation support. VHDL also represented a precise method to document the project results accepted by the European Commission.
TGI is the technology company of the TENO company, the largest industrial corporation in Spain. TGI was created in 1990 and since 1991 there have been several projects dealing with VHDL from two points of view: as VHDL users designing VHDL library components and ASICs, and as VHDL tool developers. The more relevant TGI projects related with VHDL are:

IDEAS: Development of a SPARC integer unit from VHDL to silicon. This project started in 1991 and finished between February 1994 was the first VHDL-based design project carried out by TGI. The project was partially funded by GAME. The University of Zaragoza was a subcontractor of TGI for this project. As a result, TGI currently offers commercially the VHDL SPARC compliant design database and the corresponding implementation in 0,7 mm (2MTL) by ES2 of the 32-bits microprocessor RISC core. Both products have been certified by SPARC International Inc. There is also an agreement between TGI and ATMEL-ES2 to offer the VHDL database and the chip to their customers [OI92][GGS94].

FORMAT: Formal Methods in Hardware verification. This project is partially funded by the ESPRIT III program and is focused on the development of methods and tools to formally design and verify VHDL descriptions. TGI is the coordinating partner of the project and TGI's technical work was focused in developing a formal semantics of VHDL by means of Colored Petri Nets. It started in 1992 and is going to finish by February 1996 [OLC91][OLC93a][OLC93b][OLC93c][OLC93d][OLC93e][OLC94][LOP94][OLC95a][OLC95c][OLC95f].

SMILE: SPARC Macrocells and Interface Library Elements. This project was focused on the developments of the different elements of the SPARC architecture and the methodology and tools necessary to develop embedded systems. This project was partially funded by the OMI (Open Microprocessor Systems Initiative) ESPRIT III program. It started in 1992 and finished by October 1995. The coordinating partner of this project was Matra MHS and TGI's role was to develop some peripheral cells (USARTs, Timers/Counters, I/Os, PI Bus) in VHDL that were manufactured by Matra. These models are commercially available at TGI. TGI's designs were part of the demonstrator of the project based on the SPARCLET core produced by Matra [OI93].

ESIP: EDA Standards Integration and Promotion. This project is partially funded by the ESPRIT III program. Coordinating partner is THOMSON CSF. The project started in September 1993 and will finish by February 1996. TGI's activities are focused on VHDL in Fault Modeling and Simulation. The results of this project have been submitted as working reports to CENELEC Technical Committee 117 [RI93][ENTR94][ENTR95].

SMAID: Simulation AID. It is an ESPRIT III project in which TGI is developing tools for mechanical and for mechatronics simulation. In this project a link between a VHDL commercial simulator and a mechanical one has been developed to support concurrent engineering based on co-simulation. The project started in 1994 and will finish by 1997. The coordinating partner is SIEMENS [OLC95h].

ECU: Embedded Control Unit. It is an OMI ESPRIT III project for developing tools for embedded system design based on VHDL. TGI is the coordinating partner. In this project TGI is developing a 32 bits microcontroller based on a new SPARC microprocessor core with cache memories on chip and including in the same chip a revised version of the TGI's peripheral cells developed in the SMILE project. The chip will be manufactured by mid 1996. TGI is also developing a set of tools to support hardware software integration based on co-simulation [OLC95b][OLC95d][OLC95e][OLC95g][OLC95i].

PEC: Peripheral Embedded Controller. ESA project for the development of a peripheral controller that will be connected to the MA31750 microprocessor. TGI participates with INISEL ESPACIO and the CNM (National Center of Microelectronics) in this project. TGI's
role was to produce and validate the functional VHDL test bench of the system. The chip will be fabricated by GPS. This project started in 1993 and is going to finish by mid 1996.

VAMOS: VHDL Advanced Multithreaded and Optimized Simulator. This project is partially funded by ESPRIT III special action in HPCN (High Performance and Computing Networking). This project started last January 1995 and will finish by June 1996. The University of Madrid is a subcontractor of TGI in this project. Its role is to support TGI with the multithreading version of the sequential VHDL simulator developed by TGI. This work is based on some of the tools developed by TGI in the FORMAT project. There are two prototypes of the VHDL'87 simulators, the sequential and the parallel simulators) already working and the VHDL'93 version will be ready by DAC.

There are two new ESPRIT IV projects, REQUEST and TOMI, related with VHDL and coordinated by TGI. REQUEST started last November and TOMI last December. Besides these projects, TGI is currently offering outsourcing services to design ASICs based on a VHDL design flow to several companies outside Spain.

For the majority of the Spanish electronic companies of small and medium size, usage of VHDL is made difficult as a consequence of the costs related with acquiring and maintaining of tools and the design methodology conversion costs. Nevertheless, some of them, like DIMAT in Barcelona, have made the effort and are using VHDL for FPGA design. For several of those companies, GAME has represented a way to explore ASIC design at minimum risk. Of 99 ASIC designs founded by GAME, 22 were designed using VERILOG and 6 using VHDL.

3. Usage of VHDL at the University

VHDL is being currently in the two main activities at the University, research and teaching. Most of the Spanish faculties and higher schools related with electronics (Industrial Engineering, Telecommunication Engineering, Informatics and Physics) include VHDL courses at least at the post-graduate level. During the last years some of them have made the effort to include VHDL at the graduate level in digital design and electronic system design courses.

The Universidad Politécnica de Madrid (UPM) is one of the biggest Universities in Spain. Its higher schools in the electronics area (Industrial Engineering, Telecommunications Engineering, Informatics and Physics) have included VHDL, both in the academic field and in the research and development areas, since the very beginning of the 90's. The UPM has applied VHDL in the development of several ASICs for industrial applications, being currently involved in the design of several circuits in the telecom field (DRACO, with TI+D and SIDSA), aerospace (ML/SA and ASCAT with CRISA; ESPASIC, with TECNOLOGICA), and industrial instrumentation (ENERCHIP, with Union Fenosa; ULTRATEC, with TGI). UPM is also deeply involved in the development of libraries of synthesizable VHDL components, stressing the idea of reusability (SENDA, with TGI, developing a configurable VME interface library), and in the development and promotion of VHDL based design methodologies (PRENDA, with several companies and Universities). Most of these projects have been partially funded by GAME. In the research area, UPM has been, and is currently involved in several projects related with the use and promotion of VHDL. Some of them are: ECU , ESIP, TOMI and EARNEST. The two last are new ESPRIT IV projects related with the development of tools for VHDL based design and VHDL component modeling respectively.

The Computer Architecture Group of the Informatics Department of the Universidad Complutense of Madrid has been working in high-level synthesis and system synthesis since 1988 [SMT95]. The focus of its research has been hardware allocation [SMT92], and
integration of the high-level synthesis process with low level synthesis tools [HFT93] [MFT94]. Testing aspects during the synthesis process have also been considered. VHDL is used as an interface with other tools. On the teaching aspects, VHDL is used in a Design Automation course that covers High Level and Register Transfer level synthesis with emphasis in practice.

The National Microelectronics Center (CNM) was formally created in 1985. It provides support both to Universities and companies for the design and fabrication of integrated circuits. It is composed of three branches. The main branch is situated in Barcelona. Most of the people at the IC Design Department had been working previously as a Microelectronics Design Unit in the Computer Science Department of the Autonomous University of Barcelona (UAB) since 1980. Then, by the end of 80's their natural evolution in the IC and ASIC domains brought them to learn, teach and apply the new HDL languages (VERILOG at the beginning and VHDL later). In order to disseminate these new technologies, they teach courses at the University (there are some standard courses at UAB using VHDL as a modeling tool for simulation and synthesis) and also for industry. They maintain close cooperation with the Spanish VHDL Users Group and they are also involved in projects like EUROCHIP, MEDCHIP, EUROPRACTICE (for European countries) and IBERCHIP (for Latin-American countries) that allow them to participate in and stimulate the international diffusion of VHDL and the related new design methodologies.

Their first real contact with VERILOG and VHDL was made in 1991-92 designing two small microprocessors, PL0 and ILA92 [PLM93][LMT92], for didactic purposes. The ILA processor was made in one PCB including two ASICs and interfacing with a PC-AT bus. In this project five academic groups from four different Latin-American countries were involved. Even though there were important tool limitations (only basic simulation environments for VERILOG and VHDL and no synthesis tools) the results were better than they would have been if the classical method had been followed. Later on, different people at CNM began to apply VHDL in their projects. So, at the research level, a general purpose massively parallel neurocomputer system for neural network emulation was developed. It consisted of several neurochips and offers reconfigurability, scalability and adaptability [ASH95] [SAH95a][SAH95b]. VHDL is also applied in industrial applications like the UNICORN project in which an internetworking unit to interconnect LAN's and MAN's over an ATM network based on SDH (SONET) and carrying data at the basic rate of 155 Mbits/s is being developed. 3 ASICs, 8 PLDs and 2 PCBs were involved [CTC94][CTC96][CTC96b][CTC96c].

Currently, they are involved in several complex projects using VHDL as the basic modeling and design tool. These are:

1) PEC31750: Peripheral controller for space applications. ESA project.
2) PRENDA.
3) CIMC: Multimode ASIC for mobile communications using the DECT standard.
4) NANOSAT: Communications system for low orbits satellites.

Based on the above mentioned experience they started an activity to stabilize and improve the VHDL usage at CNM a short time ago. The three main steps involved are:

1st step: Define a VHDL documentation and modeling style at CNM. This will allow them to better understand and exchange information between different teams, just using a homogeneous VHDL style and some basic tools (editors, help for documentation, etc.).

2nd step: Define and create the CNM VHDL library, including models for simulation and/or synthesis. The aim is to avoid making similar models several times and to promote a realistic module reutilisation strategy within CNM. The guide developed in the 1st step should apply to these models but the quality and acceptance criteria for the models to be included in the library would be more elaborate.
3rd step: Development of parametrisable and synthesisable VHDL module sets for application specific domains, integrating technology process information in high level synthesis. On those modules they will formalize the dependency of cost functions (area, speed and power consumption) versus architectural parameters and implementation processes. The goal is to achieve not just the specific module sets but also a good matching between estimations of cost functions at different levels of abstraction (high, logic and physical levels of synthesis) depending on architecture and technology choices.

The first and second steps are more in the development domain but the third one is more devoted to research topics. For any additional information concerning VHDL at CNM please contact Lluis Teres [lluis@cnm.es].

The CNM branch in Seville is working in two main directions: The development of Digital Fuzzy Logic Controllers and the study of timing problems. VHDL is being used not only for modeling, simulating and synthesizing Digital Fuzzy Logic Controllers [JSB95], but also a “Fuzzy Logic Package” has been developed for simulating Fuzzy Logic Systems in any IEEE Standard VHDL simulator at the algorithmic level [GJB95]. The main advantage of this is to simulate with the same tool at the algorithmic level and at the RT-level. Within their research experience in the study of timing problems in digital circuits, they developed a VHDL description of the metastable behavior of VLSI MOS latches and flip-flops [ABV93]. This description takes into account both the correct and anomalous behavior of the bistable, based on a probabilistic model.

There are very few research groups working currently in formal methods. The most important of them is the group headed by Carlos D. Kloos at the Telecommunication Engineering School of the Polytechnic University of Madrid. Their main research interests cover VHDL formal semantics [BMM96][BMS96][BSK94a], formal verification from VHDL [BSK94b][BSK95][KG96] and very high-level synthesis where they have developed HARPO, a tool able to translate a specification written in LOTOS to VHDL [GGL95][KMM95][KMR93].

4. VHDL activities at the University of Cantabria

Since 1980, the main activity of the Microelectronics Group of the university of Cantabria has been integrated circuit design in the three aspects of teaching, research and development [BVM91][MST91][BVM92][SAL92]. The availability of VHDL synthesis and simulation tools via EUROCHIP opened the way to the teaching of the language in undergraduate and postgraduate courses on digital electronic circuits and system design [GSV92].

Our research interest in VHDL started in 1990 as a consequence of our work in high-level synthesis. VHDL high-level synthesis and simulation has constituted one of our activities since that time [SR90][BSV91][CSV92][ViSa92][ViSa93a][ViAl95]. In this work, VHDL application to high-level (now behavioral) synthesis was studied and specific high-level synthesis syntax and semantics proposed. Based on this semantics, two synthesis tools were developed. PSAL2, a high-level synthesis tool [SaVi90a][SaVi90b] and FIREPS, an intelligent RT-level exploration system [TSV94]. Currently we are actively working on high-level test synthesis. The main objective is to consider testability as a design optimisation criteria, in the same way as cost, critical-path or power consumption, in order to ensure that the resulting RT architecture minimises the extra test cost [FSV93][FSG94][FSV94a][FSV94b].

As a consequence of our participation in the ESPRIT 8370 ESIP project, two research activities have been carried out. Firstly, synthesis application of VHDL where we have
analysed the current RT-logic commercial synthesis technology with the objective of overcoming the problems derived from the lack of a common, i.e. standard, VHDL RT-logic synthesis methodology [ViSa93][ViSa95]. VHDL has an unambiguous simulation semantics, supported by the ISAC and which every simulator has to satisfy. In the synthesis domain the situation is rather the opposite, no standard synthesis methodology at any level has been proposed to date and, as a consequence, each synthesis tool imposes its own synthesis methodology on the user. This fact has many disadvantages the principal one is the lack of portability. Synthesis non-portability of a VHDL description refers both to the syntax as well as the synthesis semantics of the code. Syntactical differences between tools are closely related with the different VHDL subsets and packages they support. The problem is non-trivial due to the fact that a subset will always be necessary for synthesis. In fact, there is almost general agreement in that full VHDL will never be completely supported for synthesis. Thus, a consensus is necessary in order to define a standard synthesis syntax and semantics. As syntactical errors are detected by the synthesis tool being used, this is probably the least dangerous aspect when trying to move a description from one tool to another. Semantical differences are harder, as they may lead to different kinds of implementations. In fact, as synthesis tools interpret the code in different ways, it is not ensured that the resulting hardware will be equivalent. VHDL synthesis description portability is a user need in order to ensure reusability, to allow vendor independence and to facilitate design information interchange in cooperative projects in which several departments of the same company or of different companies are involved. The main international activity towards improving VHDL synthesis description portability is led by the IEEE 1076.3 VHDL Synthesis Package Working Group (SPWG). However, the first version of the packages will cover only 10% of the model portability issue. The European VHDL Synthesis Working Group (EVSWG) leads the European contribution to the synthesis standardisation effort. The main original contribution of the EUSWG is the Level-0 VHDL synthesis syntax and semantics. In this proposal, a VHDL synthesis kernel is defined ensuring synthesis description portability to any commercial synthesis tool providing functional equivalent results. The proposal has been submitted to the IEEE SPWG as a future working topic of the group [BGV94][SeV95][VEBD94][ViDe94][ViAl95][Vi95].

Secondly, testing application of VHDL. VHDL covers all the synthesis and simulation tasks from the behavioral level down to the final implementation. Nevertheless, all the fault simulation and test generation tasks require the use of non-VHDL tools and, in most cases, proprietary description languages or notations. This has discouraged the use of VHDL in some companies as the whole design process was supported by other languages instead of VHDL. Within the ESIP project, the testing application of VHDL has been studied [EBO95][EO95] and logic-level fault modeling techniques using VITAL have been developed [BHF95]. Extension of VITAL to support current estimation, current fault modeling and, therefore, current testing has also been proposed [BSV96].

Our main research interests currently are system-level specification and system-level testing and design for testability.

5. Acknowledgments

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6. References


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