

VHDL Activities in the Netherlands.

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1. Abstract

Since the introduction of the IEEE standard VHDL (Std. 1076-1987) the use of this hardware description language and research activities closely related to it is rapidly grown.

At the presentation a summary is presented of the VHDL activities in the Netherlands.

2. Universities

From an educational point of view the three technical universities: Technical University of Delft (TUD), Technical University of Eindhoven (TUE), and the University of Twente (UT) have introduced the use of this language in their curriculum.

Also several research activities at these universities are closely related to the use of VHDL.

2.1 Technical University of Delft

In Delft alternatives for cmos logic is studied with respect to the performance (area, speed, and power). Especially focusing on the "submicron cmos technology". It is expected that the standard And-Or Invert cmos logic is not the best method for submicron.

Modelling of cmos cell including delay and power dissipation is done with VHDL. Already results with the accuracy of SPICE have been reached. The first results are published soon. For more information on this subject you may contact R. Nouta, email: reinder@cas.et.tudelft.nl.

2.2 Technical University of Eindhoven

In Eindhoven many VHDL research activities are taken place. "Is VHDL suitable for specification?" That can be seen as the central theme of their research activities.

L. Benders, and others, have presented a number of papers in sequence how to map system level specification data structures to VHDL implementation, e.g. at the European VIUF conference "VHDL-Forum for CAD in Europe" in spring 1992 in Santander. For more information you may contact L. Benders, email: leon@eb.ele.tue.nl.

Also an Interactive Design entry system is developed in Eindhoven, called IDaSS (Interactive Design and Simulation System). This system produces VHDL output as a result, that can be synthesised too. More information is found on the internet:

<http://www.eb.ele.tue.nl/proj/idasspst.html>

Or contact one of the designers of this environment A. Verschueren, email verschue@eb.ele.tue.nl

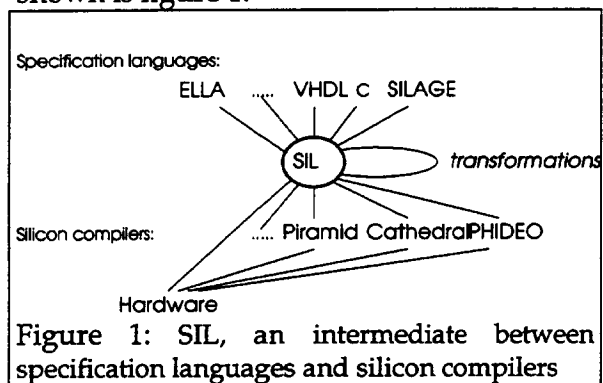
2.3 University of Twente

In Twente the research activities are focusing on the synthesis aspect of VHDL. It is well known that VHDL synthesis systems do not accept the complete IEEE Std 1076-1987/1993. The intention of it is to learn about the necessity of synthesis guidelines, or more precise their

irrelevance. Most VHDL users are familiar with the problem that a given synthesisable VHDL description for synthesis system X is probably not accepted by synthesis system Y.

For reasoning about a VHDL description an intermediate format based on single token graphs is used. This intermediate language, that is developed in the ESPRIT SPRITE Project 2260, is called SIL: Sprite Input Language [KL92].

The place of SIL in the design flow is shown in figure 1.



Currently also the generated output is VHDL again, but it is synthesisable by the commercial synthesis tools. It is synthesis tool independent, this is reached using an intermediate package that contains the synthesis tool dependent stuff. For more information on this subject you may contact the author of this paper.

3. Industry in the Netherlands

Especially the large companies, like Philips, AT&T, Océ using VHDL a long time now. Also support for the design flow in a company by developing tools for VHDL or by organising courses is done in the Netherlands.

3.1 Commercial support

3.1.1 CME

For the smaller and medium sized companies CME (Centre for Micro Electronics), a government sponsored company, gives information on the introduction of modern design flows and

has special programs to introduce (VHDL) tools in the industry.

3.1.2 Translogic

Text or a diagram entry, what is easier? Many hardware designers can design more easily using diagrams than writing text input files. A weak point of VHDL is the structural level, it is rather error prone. Translogic has developed an entry system, EASE/VHDL, that allows schematic entry and produced error-free synthesisable VHDL code.

A snap-shot of an entry window is given in figure 2. This environment is used by many companies in the Netherlands and other countries.

For more information you can send an email to info@translogic.nl

3.1.3 EDAS

EDAS (Electronic Design Automation Services) is a company that gives support on the design flow, library management and tool support (like Synopsys, ViewLogic, Analogy, A number of Mentor Graphics tools and Cadence tools etc.), and organise VHDL courses.

For more information send an email to edas@transfer.nl

3.2 Use in Industry

Many companies use VHDL in their design flow, and solved the problems they encountered.

One of the problems each company will probably encounter is library management problems. How to organise your libraries in such a way that you can easily use different tools? The support group within AT&T in the Netherlands has developed their own technique to do this. This will be public available soon.

ESA, European Space Agency, in the Netherlands has produced a large number of papers that is of interest for all designers, e.g. their "modelling guidelines" are almost famous now. It is adopted in the book "VHDL Coding Styles and

Methodologies”, Kluwer Academic Publishers, 1995. Also ESA have some advanced activities for demonstrating and evaluating design methodologies. More information on these, and more, activities see:

<http://www.estec.esa.nl/wsmwww/vhdl/vhdlpage.html>

Sometimes the use of VHDL in a company is rather surprising. EZH (a power supplier in the Netherlands) uses VHDL to design products for information transportation over the high voltage nets in the Netherlands.

4. Conclusion

In the Netherlands VHDL is really accepted as a language in the design flow of digital

systems. Also many research activities are going on, not only at the technical universities but also in the industry.

5. Literature

IE88 IEEE Standard VHDL Language Reference Manual, Std 1076-1987, Published by the IEEE, New York 1988

KI92 Kloosterhuis W.E.H. et. al., *The SPRITE Input Language SIL-1, Language Report*, SPRITE deliverable LS.a.a./Philips/Y3-M12/2, October 1992 (available at <http://wwwspa.cs.utwente.nl/aid/>)

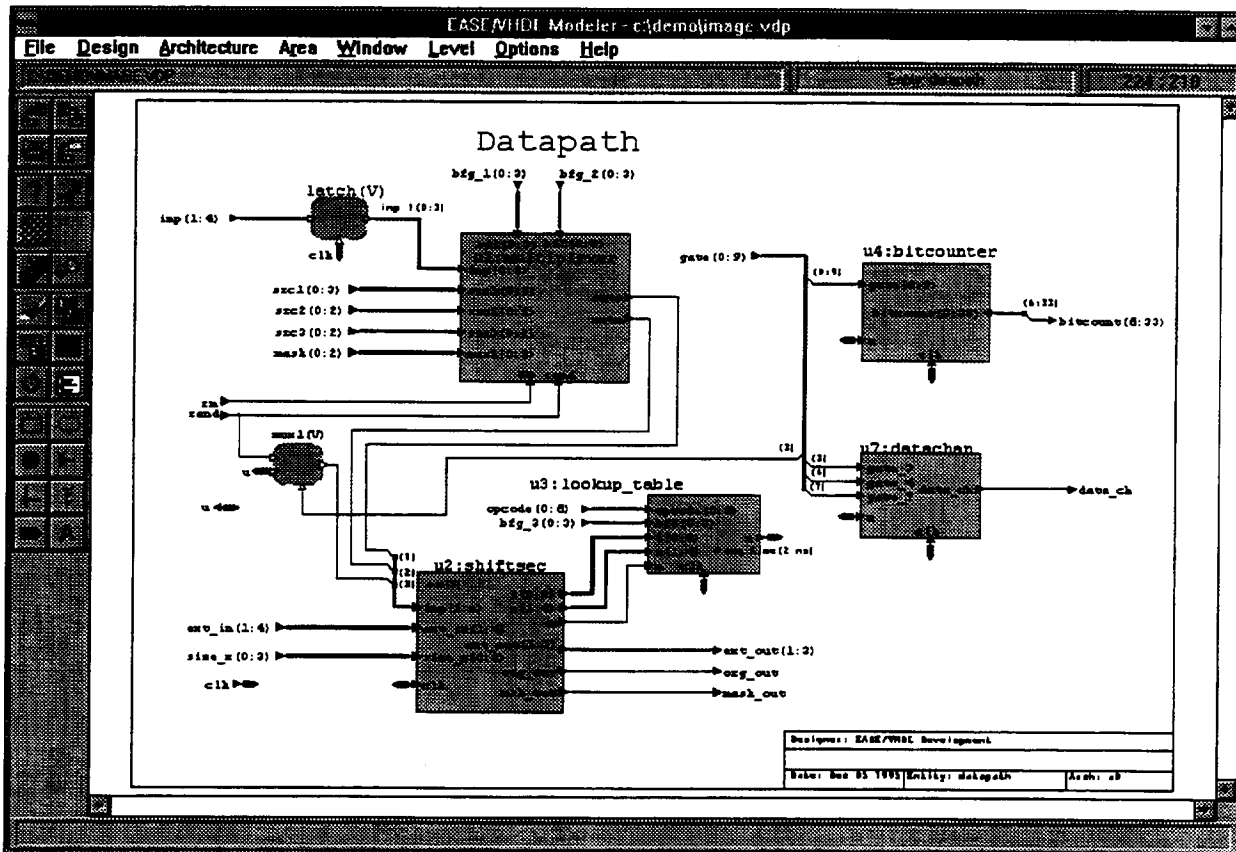


Figure 2: A snap-shot of EASE/VHDL.