Specification, Environment, and Test Plan Driven Test Bench Development

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Easily Updateable Testbenches

- A key to lowering life cycle support cost
- As a system evolves, model testing requirements frequently change
- Model tests are encapsulated in the testbenches
Premise
Testbenches should:

- Be automatically driven by specification requirements
- Accurately reflect the system environment
- Be configured by a test plan

Approach

- Use existing tools as much as possible
- Tool types:
  - Code Generators: develop testbench code from high level, graphics based models (Ilogix-Express VHDL, SPW, Ptolemy, COSSAP)
  - Environmental Data Generators: SPW, xpatch, IRTOOL, and IRAMP data base.
- Required knowledge cuts across traditional engineering boundaries
Two Applications

- SAR: model radar signals
  - transmission, return delay, down converting, deramping, and type conversion
  - one dimensional test case
- Infrared Search and Track: model pixel arrays
  - target image, background clutter, merging, noise injection
  - two dimensional test case

Specification Repository

- High level system block diagram
- Blocks correspond to real system components, underlying VHDL hidden.
- Implemented with a commercial schematic capture tool (Synopsys SGE)
- Specification parameters are symbol attributes
- Parser extracts specification values & feeds them forward to Test Bench Generator
Accurate Environmental Modeling

- Principles:
  - Use tools specific to the physical environment
  - Convert data formats to those required by the test bench
  - Employ strategies for reading and manipulating large arrays of data

IRST Environmental Modeling

- IRTOOL (Arete’)
  - Infrared returns from selected object shapes
  - Format conversion from HDF to ASCII
- IRAMP
  - data base of clutter files maintained by NRL
  - two dimensional images of sea & clouds
- Sensor noise and dropout
- Data loading times: 10 sec
SAR Environmental Modeling

- SPW real number model of transmission, return delay, down converting, deramping, and format conversion
- Superposition of simple object returns
- Also data files from MIT, Lockheed, and xpatch
- Memory storage and read time for large files
Test Plan Interface

- Test plan: a document which organizes system requirements in terms of how the requirements will be tested.
- Requirements divided into groups, a set of tests is allocated to each group.

Library Based Testbench Construction

- For each application (SAR or IRST), the testbench is an unbound, structural architecture.
- Each test is mapped to a VHDL configuration body of that architecture.
- Configuration body specifies which library to component to use and assigns values to generics.
- Test groups correspond to partially specified configurations.
Testbench Component Libraries

- SAR:
  - High level: Genchirp, delay, downconverter, deramper, decimate, merge, noise
  - Low level: chirp, complex tone, complex multiply, delay, complex conjugate, decimate, type conversion
- IRST: target, clutter, sensor, clock

Demonstration SAR Test Plan

- Evaluate the range of a point target
- Evaluate the range of multiple point targets
- Evaluate resolution of SAR MUT.
- Evaluate SAR algorithm noise sensitivity
Testplan 2
4 targets at range bins of 476,869,1131,1787. (Ranges of 7140,7230, 7290,7410 m.)

Testplan 3
Reference target at 7260 m (range bin 1000)
2nd target at 7260.19 m (range bin 10002)
(can be resolved)
A test case of Testplan 4 (with Gaussian noise of $\sigma=9.4$) SNR=-35dB
(when $\sigma>=9.5$, the post filter reports ghost targets)

Demonstration IRST Test Plan

- Simple target detection
- Target detection with platform motion
- Target detection with sensor gain variations across the array
- Target detection with sensor noise
- Target detection with background clutter variation.
Systems Integration Work

- Existing design and application area tools can be used to develop pieces of a testbench.
- Two software systems integrate the pieces:
  - Test Bench Generation System
    - User Interface: TBGUI
  - VHDL Test Simulation Controller
    - User Interface: TBEUI
Modeling Support Tool

- Modeler's Assistant
- Models constructed from Process Model
  Graph and Process Primitive Library
- Provides for process level code reusability
- RASSP processes primitive libraries for
  IRST and SAR
- Tool available through WWW site:

PMG of SAR Sensor (MODAS)
Conclusions

- Effective testbench generation requires:
  - Automatic linkage to the system specification
  - Accurate environmental modeling
  - A test bench component library
  - A test plan interface to configure the test bench structural architecture

- Commercial tool suite used for generation of test bench pieces.

- Software systems developed for test bench generation and simulation control