

# Integrating VHDL Into Electronic Technical Data Package Specifications

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## Abstract

There has been a profusion of electronic standards in recent years for the design, description, specification, and simulation of electronic hardware systems and sub-systems. Such standards include VHSIC Hardware Description Language (VHDL), Waveform and Vector Exchange Specification (WAVES), Electronic Data Interchange Format (EDIF), and Initial Graphic Exchange Specification (IGES) among others. Although these standards enhance engineering productivity and product integrity, a need still exist for an integrated environment for electronic hardware descriptions and specifications which incorporate these standards. The benefits of such an environment include:

- technology independent data package descriptions
- an electronic vs. paper documentation environment
- user friendly interface for accessing specification information

This paper presents an Electronic Technical Data Package (ETDP) methodology for the development of a cohesive EDA framework, required to capture all of the critical data necessary to support engineering redesign functions an requirements at the microsystem level.

## Introduction

The primary purpose of the Microsystems Prototyping Laboratory of Mississippi State University is the establishment of a VHDL center of excellence to address current and future government and industry research and development needs in the area of VHDL modeling, model verification, and in support of the primary function of microelectronics obsolescence. The ETDP methodology development demonstration project addresses the need for a unified framework in support of microsystem redesign methodologies.

VHDL modeling of the behavior and structure of existing systems will yield specification models which form the basis for ETDPs. The VHDL simulation models comprising the ETDP create a non-ambiguous description of the electrical behavior of the system. A printed circuit board (PCB) that provides a realistic microcircuit obsolescence scenario where the preferred solution is to replace the original PCB with a redesigned PCB, designing out the obsolete circuits, will be used to illustrate the ETDP concept.

## Diagnostic Panel Interface (DPI) Microsystem

The example PCB includes structural VHDL descriptions for both the original and reengineered printed circuit boards. The original PCB represents a dated technology SSI microsystem implementation. The redesigned PCB contains an ASIC replacing approximately 90% of the original circuit. VHDL models and test information exist for both PCBs. Both VHDL architectural descriptions share the same I/O and generic interface and WAVES test environment. A high-level structural view of the VHDL model specification for the microsystem is shown in Figure 1.

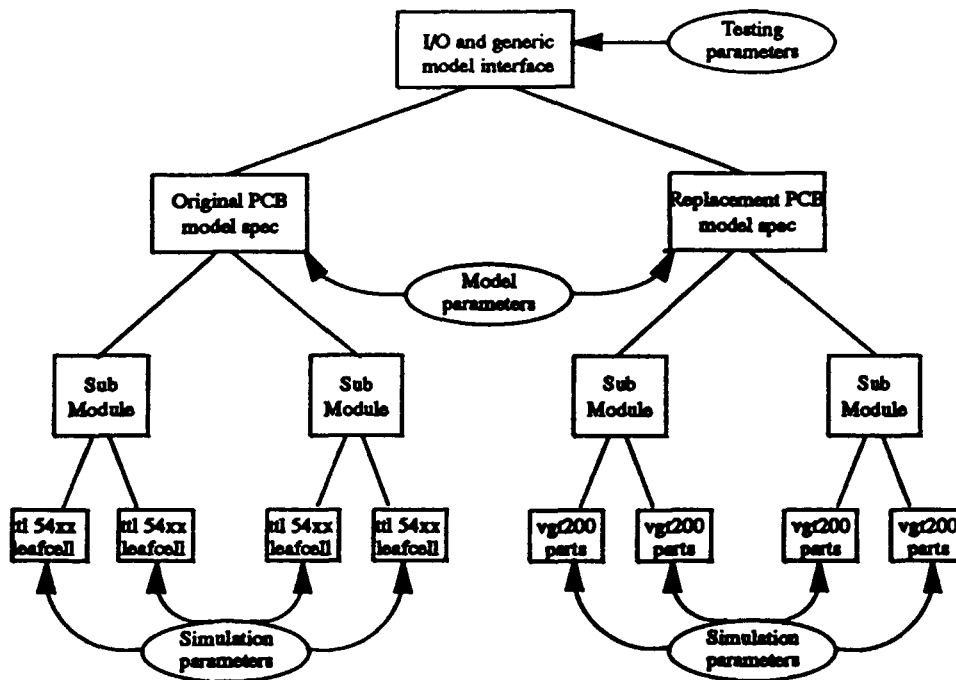


Figure 1 : Microsystem PCB Structural View

The VHDL structural implementation of the original design consist of approximately 60 leafcell instances that are distributed between 13 sub-modules. The reengineered design is a gate-array implementation consisting of several hundred cell instances. WAVES test benches and test vector suites exist for each sub-block and leafcell that make up the design. Additionally, parameters that affect model timing (simulation parameters) may be set at the leafcell level. The model parameters allow the user to set up system clock information.

### Electronic Technical Data Package Approach

The idea behind ETDPs is to provide the user with a flexible configurable environment for *viewing* technical data associated with microsystem designs. Additionally, the burden of managing and maintaining the database view hierarchy is transferred from the responsibility of the user to the ETDP application. The initial ETDP concept encompasses the ability to *kick-off* CAE applications software when a specific view of the microsystem hierarchy is requested. These CAE applications are intended to be run in a *view only* mode and do not support any type of editing capability. There

are a multitude of data package views which can be incorporated into an ETDP. Currently, there are three types of specification data that the user can access via the ETDP application:

- |                                     |                           |
|-------------------------------------|---------------------------|
| 1. VHDL Simulation Models           | <i>Simulation View</i>    |
| 2. Graphical Schematic Capture Data | <i>Schematic View</i>     |
| 3. Technical Documentation          | <i>Documentation View</i> |

Figure 2 illustrates the View concept. The ETDP application (represented by the first oval) establishes a link to the various CAE database components which represent the various views of the data package.

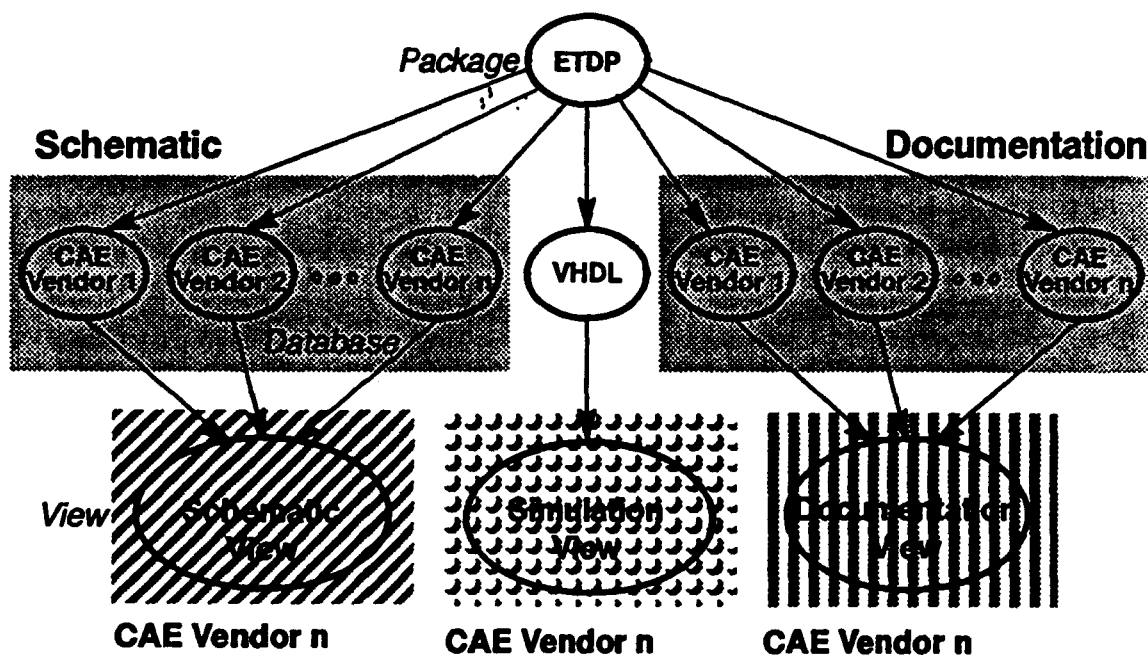


Figure 2 : CAE Vendor Database/Tool Dependence

These views are then called up via interface commands from the ETDP application which can then kick-off desired CAE tools in order to display a particular view of the package.

### Viewgen

Viewgen is the ETDP application which binds the components of the technical data package into a cohesive and manageable framework. The first step in building an ETDP environment involves the generation of a view specification for the design. The view specification is generated via a formal grammatical definition and list all of the components available for the ETDP application. A partial listing of the view specification for the example DPI microsystem design is shown in Figure 3. The key-words for the view specification are highlighted in bold type. Note that the VHDL simulation parameters (supported by the simulation view) that the user may select are

listed as part of the view specification. Aside from serving as a documentation tool, the view specification also defines the view hierarchy for the microsystem database. The ETDP view specification is flexible enough such that multiple views of the same ETDP environment may be defined. These views may include hierarchical views, flattened views, or some combination in between. For example, if test benches and test vector suites did not exist at the block level for the example microsystem, the simulation view for the sub-modules would be omitted. The ETDP application also incorporate mechanisms for defining dependencies between the various components that make up the ETDP for a particular microsystem.

```

VIEW DPI {
  VIEW DPI_Original {
    PARAMETERS global_flags Sim_Params (
      ENUMERATION time_mode (MINIMUM, TYPICAL, MAXIMUM, GENERIC),
      STD_ULONG, initialize_outputs, BOOLEAN X_gen, BOOLEAN Time_Mesg,
      REAL Vcc RANGE 4.5 TO 5.5, REAL Ta RANGE -55 TO 125 );
    PARAMETERS DPI_test Test_Params (
      STRING Test_Suite ("pwrdown_test", "functional_test_A", "functional_test_B"),
      TIME Period, REAL Tolerance RANGE 0 TO 1, BOOLEAN Compare,
      SEVERITY_LEVEL Assert_Level, ENUMERATION Print_format (standard, WAVES));
    PARAMETERS HSC_circuit Model_Params (
      TIME clk_period, BOOLEAN Delay_Select );
    SCHEMATIC DPLsch
    DOCUMENT Critical_Paths.doc
    VIEW Q_Block {
      PARAMETERS global_flags Sim_Params
      PARAMETERS Q_Block_test Test_Params
      SCHEMATIC Q_Blocksch
      VIEW SN54S280 {
        PARAMETERS global_flags Sim_Params
        PARAMETERS SN54S280_test Test_Params
        DOCUMENT SN54S280_datasheet
      }
      VIEW SN54S04 {
        PARAMETERS global_flags Sim_Params
        PARAMETERS SN54S08_test Test_Params
        DOCUMENT SN54S04_datasheet
      }
    }
  }
  VIEW DPI_Replacement {
  }
}

```

**Figure 3: DPI View Specification (Partial Listing)**

In addition to the view specification, the ETDP application requires additional information for binding the different views to their host environment. This is accomplished by generating a set-up file that contains the required information. This file contains an entry for each view in the view specification. For example, an entry for a simulation view contains six fields with the following format:

- |                 |  |
|-----------------|--|
| 1. logical name | used for view look-up                                |
| 2. file name    | the package or configuration declaration source file |
| 3. file type    | key-word PACKAGE or CONFIGURATION                    |
| 4. search field | package name or binding indication                   |
| 5. analyzer     | analyzer command string                              |
| 6. simulator    | simulator command string                             |

By uncoupling the platform and tool specific information from the view specification, the view specification can remain static across multiple database environments.

Once the view specification and set-up file have been defined for the microsystem, the next step is to generate the user interface for view access.

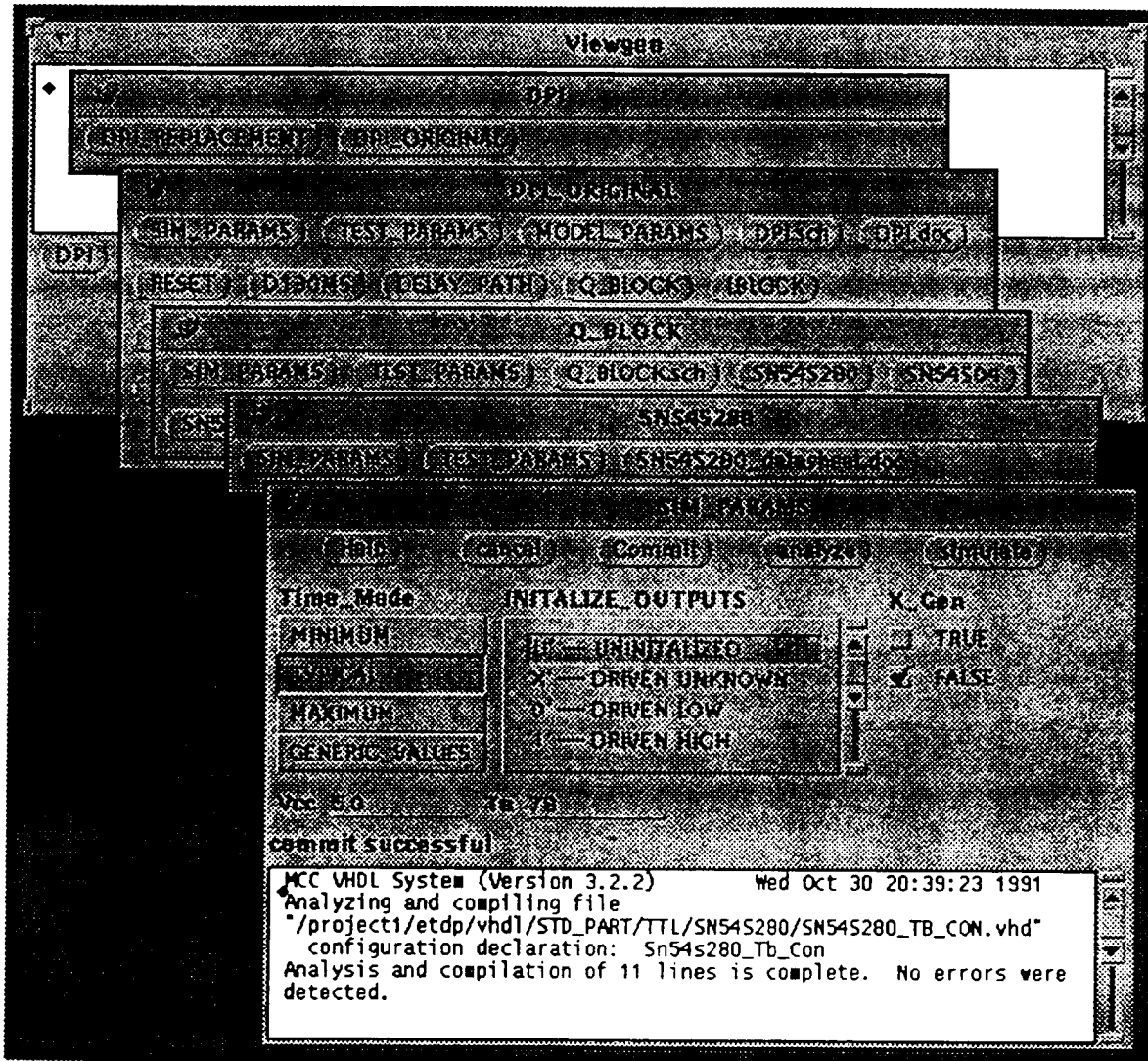


Figure 4: DPI Viewgen Interface

The interface is generated dynamically via the ETDp applications software by parsing the view specification and set-up files. Figure 4 shows the user interface for the DPI microsystem in an

active screen configuration. The first panel represents the apex of the DPI view hierarchy as defined by the view specification. Subsequent windows represent the descending levels of the DPI view hierarchy. The last window represents one of two VHDL simulation views for the SN54S280 leafcell which is a component of the original DPI printed circuit board.

The Viewgen ETDP interface software and utilities were developed under the OPEN LOOK User Interface. The OPEN LOOK UI was chosen for this demonstration as it offers some significant advantages over other user interface environments. These advantages include:

- good visual design
- device/platform independence
- interoperability with other popular user interfaces

### Conclusions

The Electronic Technical Data Package Methodology developed in this project provides a vehicle for the demonstration of the use of existing CAE tools to capture all behavior and documentation associated with the specification and redesign of a printed circuit board. This project clearly demonstrates the value of electronic media documentation, VHDL microsystem specification, and VHDL redesign as applied to the solution to an example obsolescence problem. In addition, database techniques will be explored and developed to create an environment to facilitate the generation and management of specific ETDP applications.

### Future Work

Phase II of the ETDP Methodology Development will consist of creating an ETDP environment which displays desired package views from a unified database where all of the data is captured in accepted government, industry, and university CAE standards.

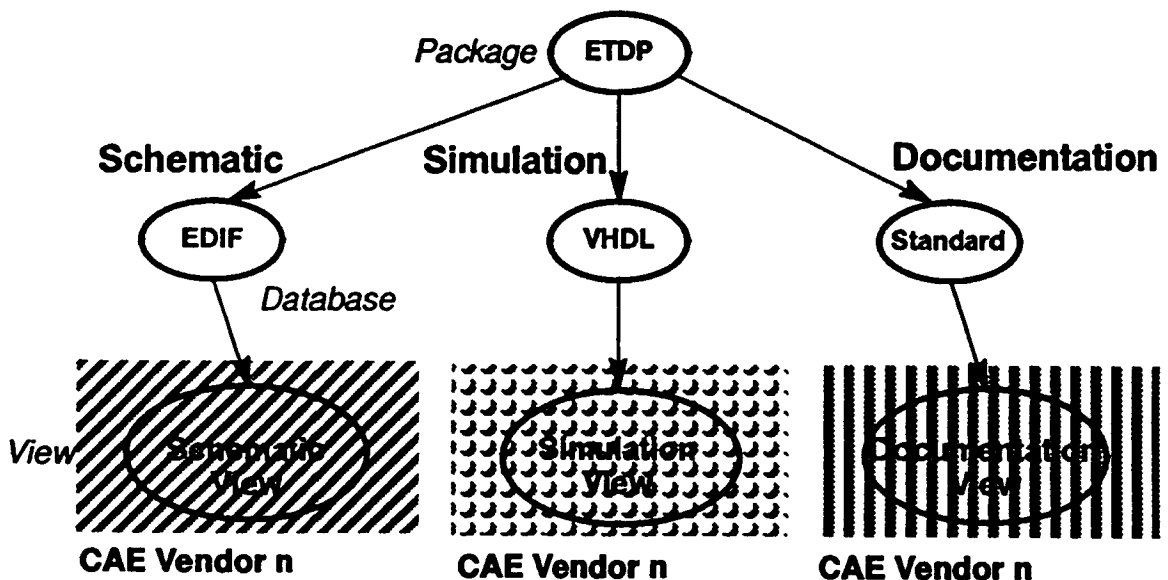


Figure 5: ETDP Phase II - CAE Vendor Database Independence

VHDL represents one of these accepted standards (as depicted in Figure 2) and as others are added (EDIF, etc.) the database comprising the ETDP will migrate to a standards database that will allow complete portability. Figure 5 illustrates the Phase II ETDP concept.

The third and final phase of the ETDP Methodology Development project will be to examine the usefulness of developing a standard ETDP View Package. The use of CAE vendor packages for displaying desired ETDP packages views is not only convenient for developing the ETDP concept but adds the additional advantage of displaying the data in a tool format familiar to the user. However, utilization of this display concept is very much an overkill usage of the target CAE tool because of the *read-only* nature of the data. Also, to display Phase II ETDP views requires a CAE vendor package for each desired view of the database. This is fine for design organizations (a primary end user of ETDP technology) which already have resident a complete set of tools, but may be unpractical for organizations interested only in viewing the data. Therefore, Phase III of this project will explore the development of a standard viewing tool which will access the entire ETDP database structure and display the desired view in a standardized fashion. Figure 6 illustrates the Phase III ETDP concept.

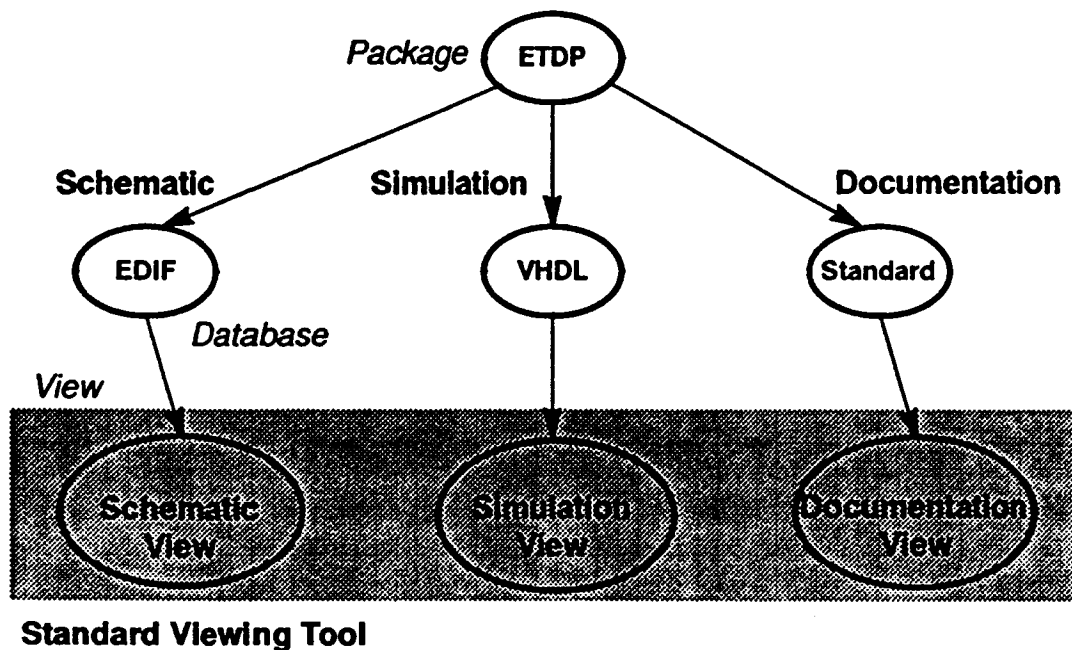


Figure 6: ETDP Phase III - CAE Vendor Tool Independence

### Acknowledgments

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