

## VHDL Modeling Standards – Present and Future

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### **Abstract**

Modeling represents the last frontier of standards in the VHDL marketplace. VITAL and OMF model packaging are representative of the present and future of this frontier. The VITAL standard is an official IEEE standard and the ASIC and EDA vendors are beginning to adopt it. OMF model packaging is rapidly gaining momentum toward becoming the standard for distributing IP. However, standards are only useful if there is broad market acceptance of them. A brief history of both standards will be presented. The histories will be followed an exploration of the current market condition and an extrapolation of the future of these standards.

### **The Age of Innocence**

VHDL was conceived as a documentation language, but grew as a simulation language. The language was formed by the United States military as a standard means by which military contractors could document digital designs. The language provided constructs to support both abstract and detailed digital design. As companies documented their designs in VHDL, the early VHDL simulators provided a means to verify that the circuit was documented correctly. Companies quickly realized that they could apply the “documentation verification” earlier in the design process and thus began to design with VHDL.

When designers began to implement designs with VHDL, the limitations of the 1987 standard became apparent. Built into VHDL is a simple binary data type. However, designers needed several logic states to accurately model digital circuit characteristics. As designers applied VHDL to ASIC and IC design, the limitations in terms of gate-level modeling became apparent. VHDL needed to mature into a design language in order to gain more wide-ranging support.

### **The Rites of Passage**

In the early 1990's, it was clear that the VHDL marketplace needed to add design oriented standards in order to enjoy the growth seen in the Verilog marketplace. The first such standard was the IEEE 1164 standard for multi-valued logic. This gave designers a standard means by which to accurately model circuit characteristics. This standard package rapidly spread through the simulation and synthesis tools. While designers found improved ability to reuse designs, 1164 did not improve the availability of ASIC and FPGA libraries.

Multi-valued logic alone was not enough to stimulate significant growth. This growth had to come from the largest consumers of VHDL based EDA technology - ASIC and IC designers. The catalyst for movement in that market was the availability of standard gate libraries. The 1995 VITAL standard, IEEE 1076.4, resolved this issue. It provided for standard backannotation, timing, and functional modeling in a manner similar to Verilog. Most importantly, ASIC vendors could produce a single VITAL library that all VITAL compliant simulators could simulate, and possibly accelerate.

With these standards in place, the VHDL marketplace is approaching the size of the Verilog marketplace. According to the EDAC market statistics, the 1995 market for VHDL-based simulators was \$53 million and for the Verilog-based simulators was \$73 million. While these numbers seem encouraging, analysts have declared "this is the year that VHDL will overtake Verilog" for at least the last three years. What will it take for the VHDL marketplace to grow further?

### **Ready, Set, Grow!**

The factors that will propel the VHDL marketplace are coming together. VITAL library availability, OMF high-level modeling standards, and third party debugging tools together will create a compelling solution. These factors, combined with the inherent strong typing and levels of abstraction in VHDL, will energize the marketplace in 1996.

Every month brings several more VITAL sign-off announcements from the ASIC vendors. Many of these vendors have experience with Verilog and have only begun to work with VHDL after the VITAL standard was established. Following sound business practices, the major VHDL simulation vendors have been actively supporting the development of VITAL libraries through training, services, engineering support, and library translation. To date, more than 30 ASIC and FPGA vendors have announced VITAL libraries. The next step to accelerate VHDL's expansion is for EDA companies to use these VITAL libraries for timing analysis, test generation, layout verification, etc. With the back-end design covered, designers will be able to capture, verify, synthesize, and build their designs completely in VHDL.

The dream of full board or system simulation still eludes many VHDL users. In almost every instance it is the lack of available models that prevents board level simulation. In some cases the available bus functional model does not provide the detail the designer needs, but the IC vendor can not distribute a more detailed model because of the risk to the security of the IP. The VSI (Virtual Socket Interface) Alliance, RAPID, and the Open Model Forum are working on the model standards for authoring and distributing IP. When the standard for the socket is adopted, and the EDA vendors build it into their simulators, the packaged IP will be useable on a variety of simulators. This will not only support board level design, but it will support ASIC design as well. ASIC vendors have been distributing pre-designed "cores" in Verilog or VHDL and are in desperate need of a means to protect their IP. These include units such as PCI controllers, MPEG decoders, and MPUs. ASIC and IC designers add their own IP in the same manner that PCB designer adds PLDs and FPGAs to a board that contains microprocessors, UARTs, and memories. Another proponent of full board or system simulation is mixed VHDL and Verilog simulation. Several EDA vendors offer these mixed-language products today. Thus, a designer is able to choose VHDL as a primary language and still achieve system simulation, even if some of the models are Verilog based.

The last factor for increased growth for VHDL are third party tools. These complete the debug environment for customers. Data management tools, waveform viewers, code profilers, backplanes, and other tools make up this segment. These tools began to emerge for Verilog soon after it was released into the public domain in 1990. For VHDL, this market has been growing more slowly. However, compelling events, such as VITAL's acceptance, have accelerated the growth. The future is bright here as customers demand more high-level capture tools, debugging environments, code analyzers, and test bench generators. The growth in the third party market and the growth in the core VHDL simulation market feed one another.

### **Conclusions**

The VHDL marketing place is poised for strong growth. However, that growth has depended, and will continue to depend, on the timely adoption of standards. The history of VHDL contains many examples of growth being driven by standards events. 1996 and 1997 will yield standards for modeling that will broaden the appeal of VHDL and allow its rapid application to deep submicron and complex PCB applications. Further in the future is the need for mixed-signal on chip, especially for multimedia and telecom applications. Quickly resolving issues with the analog version of VHDL will provide a rapid response to this market need. With continued focus on standards, VHDL will be the overall design standard.