

Emulation Speeds Verification of 3D Graphics Accelerator

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Abstract: This paper provides a user case study that shows how the complexity of designs and competitive factors in the 3D graphics market require application specific verification methodologies in order to meet time-to-market, performance and cost objectives. The article will describe the experience of designing the hardware and software for a 3D graphics application called "3D-Master" by SP3D, a joint venture with Philips. traditional and non-traditional verification methodologies will be contrasted from the standpoint of cost, performance, and results along with the investment in time and resources involved to implement application specific emulation as a key differentiating technology of the non-traditional flow. Results will be examined from the point of view of cost/benefits and ROI with a particular focus on the unique value provided by emulation vs simulation.

Introduction: Managing design complexity is becoming more challenging in the face of widely available sub-micron manufacturing capabilities, top-down design and the demand for the fastest time-to-market. As a result, the need for higher levels of design abstraction has become a key issue in sub-micron designs.

Sub-micron manufacturing capabilities enable single chip to be designed with over one million gates. As a result design methodologies have shifted towards higher levels of abstraction and involve concurrent hardware/software development. Today's design teams are therefore staffed by hardware and software designers, both working in parallel on firmware designs.

Especially, in developing graphics systems for multi-media applications it is very important to have short development cycle so that the time-to-market requirements and small product windows can be met. At the same time complexity of designs has grown significantly because not only the basic graphics features of 2D graphics have to be implemented but also 3D graphics acceleration (MPEG Decoding Etc.) have to be implemented.

Goals and Objectives of the 3D-Master Project: SP3D recently completed the design and prototype of the "3D Master" which is a high performance graphics accelerator for low cost PC systems. The 3D-Master device is a 120,000 gate, cell based ASIC with 16 Kbits of internal memory manufactured by Philips using it's C100, 0.5 micron technology. This chip is expected to provide the advantage of PCI bus "plug-and-

play" by enabling 3D-only graphics PCI boards. Primary objective behind 3D-Master was to allow PC users to preserve their investment in existing 2D graphics boards and to offer a cost effective alternative supporting 3Dgraphics to OEMs of low cost 2D SVGA motherboards.

SP3D's objective behind the 3D-Master chip were:

1. To render flat and Gouraud-shaded, textured triangles with Z-buffering and blending for color depths of 8, 16, 24 and 32 bits.
2. To perform source or destination blending with transparency support for color keying, hardware dithering, stencil test and buffering, and anti-aliasing with super-sampling.
3. To obtain a performance of 50 million pixels/second and 100K polygons/second with Gouraud Shading and Z-buffering enabled.
4. To design a PCI bus master interface into the accelerator ASIC to copy the rendered picture from the local rendering buffer to the frame buffer of 2D graphics boards.

Entire ASIC was designed in VHDL and an application-specific verification approach was chosen to keep the verification cycle to less than 3 months.

Traditional Verification Solutions and Limitations: While verification of such ASIC designs is traditionally accomplished through simulation, first at the RTL-level and then at the gate-level, the complexity of graphics accelerator application required different strategy to reach the market on time.

For verification of the whole chip, it was necessary to render millions triangles of different sizes and all possible color depths. This led, in combination with enabling or disabling the features of 3D-Master, to a huge battery of tests. The results of these test runs must be compared with the output of C-model of the design. Depending on the screen resolution and the number of triangles to be processed, the simulation time varies between half an hour to six or more hours for each test. Verification of full 3D-Master with software simulation alone would have taken over a year which was not acceptable.

Hardware simulation accelerators were one alternative that was considered to speed up the verification process. These systems accelerate simulation, maintain same user interface and run the same testbenches as software simulators. Eventhough, accelerators offer 100X performance improvement over software simulators, they are still dependent on testbenches generated by designers. Also one of the fundamental verification requirement was ability to develop and test driver software for the chip in parallel with hardware verification.

Hardware emulators, that substitute for the final chip in the target system was another alternative. With an emulation, the software simulation testbenches are replaced by the real target system which makes it possible to test the design in its real environment, and provides an advantage of finding bugs or incompatibilities that may otherwise not be found using traditional software or hardware-assisted simulation.

SP3D decided to use an emulation for the 3D-Master project because it allowed designers to not only verify the hardware design itself, but also develop and test the driver software for the chip simultaneously in a hardware/software co-verification environment with a simulation only solution, test of the driver software can not start before receiving first silicon, so it is impossible to shorten the design cycle by overlapping hardware-software development.

SP3D selected Quickturn Design Systems, System Realizer™ product line as an emulator of choice because it gave the flexibility to verify the design directly in its natural environment - the PC. The System Realizer uses an array of Xilinx FPGAs to build a system that behaves, except for the timing, the same as the final chip.

Design Methodology: Before starting emulation entire design was verified at the module level using Cadence's Leapfrog simulator. A short Leapfrog simulation at the top-level was performed to verify the basic functionality of the design and to eliminate bugs in the early phase. The design was synthesized using Synopsys's Design Compiler. The final gate-level simulation was carried out only for verifying the timing constraints before and after the chip layout. An EDIF netlist is automatically partitioned using Quickturn's emulation software to fit an entire design into an array of Xilinx FPGAs inside the System Realizer. The design is then compiled to generate bit pattern which is downloaded into System Realizer in a matter of seconds. An emulator can also be used as an accelerator to validate vectors obtained during simulation

.Verification Challenges Using an Emulation: An emulation system runs between 0.5 MHz to 4 MHz which is much slower than the final chip. This mandates designers to slow down the target PC system. An ASUS SP3G motherboard was chosen that included an Intel 486 CPU, PCI bus, SCSI port, IDE port, serial and parallel ports. The on-board oscillator was disconnected and external clock was supplied to the PC.

Major challenge in slowing down the PC was to keep the dynamic parts such as RAMs running correctly. However, memories were refreshed often enough to maintain values. The only part of the PC that failed to work at lower frequencies was the floppy disk drive. This was overcome by performing data transfer via network.

To mechanically connect an emulator to the target PC, an emulation board that is pin compatible to the final chip was developed. SP3D leveraged one board for verifying both the design and the first silicon prototype in the same system environment. For emulation a special QFP240 connector was provided by Quickturn.

Netlist Optimization: Since an emulation only verifies the functionality of your design and not the timing, SP3D performed an extra synthesis run without timing constraints that finished overnight. In contrast, full synthesis run with all constraints lasted three days.

To implement 3D-Master's internal RAM, memory compiler was used to target memories on FPGAs. The emulation shells provided a clock for the write enable pulse for the RAM. This is a time-intensive part of the netlist transformation process. 3D-Master memories were distributed into several FPGAs. Though using this emulation feature proved somewhat tedious, it dramatically improved an emulation gate-utilization.

Compilation of the synthesized, gate-level netlist into an emulator internal format took another night. So total turn-around time of two days is achieved for finding a bug in an emulation to verifying a corrected netlist. On first impression, this seems like a very long time but the amount of data processed during emulation would require much longer turn-around time if simulated. With simulation designers would re-simulate after every change in the netlist, whereas an emulator supported an incremental changes.

In-Circuit Debugging: After correct transformation of the gate-level netlist, "In-Circuit" emulation was started to run tests and search bugs in the design's natural environment. An internal test software was used for initial tests. In addition some higher-level software was concurrently tested with the hardware.

Rendering problems are generally obvious to see with an un-trained eye. Several bugs were detected in-circuit by visually inspecting the displayed pictures on the PC screen and comparing them against a reference image on a workstation monitor. To ensure bit-true verification, contents of different chip buffers (rendering buffer, Z-buffer etc.) were saved to a disk for comparison with the results of a C-model. An in-circuit emulation enabled verification using a large library of more than four hundred still and moving pictures through the 3D-Master at high resolution (640X480 pixels X 32 bit color). Traditional simulation would have enabled small images at low resolution in the same amount of time.

Several bugs were found during an in-circuit emulation using Logic Analyzer built-in an emulator. One limitation to this approach was one can observe signals at FPGA boundaries. However, an analyzer software does provide a capability to set extra probes which connect internal FPGA pins to free pins at the FPGA boundaries. This was performed incrementally to the existing design or during a full compile if there were not enough FPGA pins free at the desired observation point.

Upon completing an emulation phase of the design cycle, two major rendering bugs with very specific triangles were detected that were simply not possible to detect with traditional simulation techniques. An in-circuit emulation was also useful for detecting incompatibilities with the PCI standard for which work-around had to be developed in the form of a new version of the system BIOS to correct the PCI incompatibilities.

Emulation results were as expected, except for the extra time required to set up RAMs and lack of visibility into FPGA internal signals. This problem has been resolved by Quickturn's next generation emulation software called QuestII. The QuestII also provides super-fast RTL mapping tool that directly maps VHDL/Verilog RTL description to an emulation database.

Summary: Overall SP3D saved several months of time and avoided the significant cost of re-design using an emulation. The verification time was shortened and software was ready a few months earlier than it normally would have been using a traditional verification flow. During chip fabrication, software developed continued using the emulated design for debugging.

At the end, it was possible to produce still pictures and short animations. Although, it was much slower than the design in silicon, it was impressive to see the performance made possible by an emulator. The single most important result and evidence of our success with an emulation was that the final 3D-Master silicon behaved identically to an emulated design.