

MULTIPLE VHDL TOOLS IN THE DESIGN ENVIRONMENT

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1. Abstract

VHDL is becoming the most frequently used design language for both simulation and synthesis. Some of the major factors in selecting VHDL tools are speed, efficiency, cost, and user friendliness. In our design group, multiple simulation and synthesis tools were chosen. While the main goal of VHDL is to make designs portable, today's environment does not allow this to happen. Using multiple tools in the same design environment caused several problems for the users. Considerable effort were spent in selecting the libraries to be used as well as the data types. This paper describes the reasons behind the multiple tools environment, the steps taken to provide a user friendly environment, and the experiences learned from it.

Keywords: VHDL Simulators, VHDL Synthesis, Interoperability, Standards.

2. Introduction

The number of CAD (Computer Aided Design) tools supporting VHDL (VHSIC Hardware Description Language) simulation and synthesis has grown to complete tool sets for synthesis and simulation. Several factors are involved in selecting a CAD tool, technical factors such as speed of simulation, accuracy, robustness, and libraries and packages supplied by the vendor and non technical factors such as price, service, availability, ease of use, and other human factors. In today's market all these requirements are not available in a single tool. Designers have to choose the tools based on the most important criteria in their environment or accept the existence of a *multi-tool environment*.

3. Tool Selection

After a period of evaluation in which several VHDL simulator and synthesis were evaluated the following tools were selected. For simulation

VSS from Synopsys was selected because of robustness, ease of use, debugging capabilities, and familiarity to several designers [1]. Also, V-System from Model Technology Inc. (MTI) was chosen as the basic simulator because of simulation speed, price, and being integrated with ATTSIM which allows mixed C, VHDL, gate level, and mixed mode simulation [2] [3]. For synthesis DESIGN_ANALYZER from Synopsys was chosen because of quality of synthesis for ALU/Arithmetic circuits and familiarity [4]. While SYNOVATION from AT&T was chosen because of quality of synthesis for state machine based circuits and for price [5]. This creates four environments described in the following table:

Table 1:

| Environment | Simulation Tool | Synthesis Tool |
|-------------|-----------------|----------------|
| 1 | MTI | SYNOVATION |
| 2 | VSS | SYNOVATION |
| 3 | MTI | SYNOPSIS |
| 4 | VSS | SYNOPSIS |

4. Multi-Tool Environment Problem

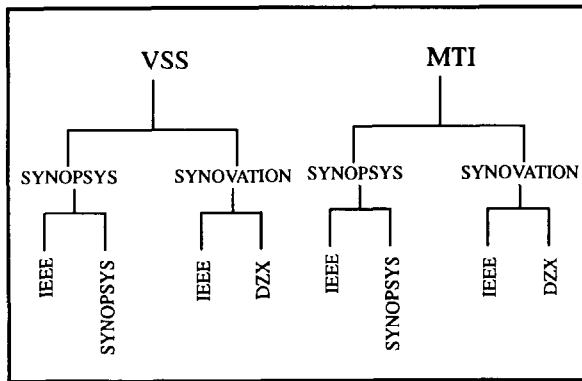
Current IEEE (Institute of Electrical and Electronics Engineers) standards are limited to a basic set of data types and functions. The basic set of libraries and packages were standardized in 1987 and they were later augmented in 1993. Since the main goal of VHDL was to provide a standard environment that allows portability of designs and not having to worry about tool specific requirements, having two different tools should not represent a problem. However, until now each vendor defines which standard logic (std_logic) packages go under the IEEE library and which packages belong to a tool specific library. Some of the std_logic packages are *std_logic_signed*, *std_logic_unsigned*,

std_logic_arith, and *std_logic_textio*. Synopsys puts the *std_logic* packages under IEEE while AT&T puts *std_logic_1164* only under IEEE and the remaining packages under the *dazix* (DZX) library. Also, other functions and operators are named differently. Examples are the shift operators, methods of inferring a specific type of flip flops, and type conversion functions.

Because of the difference in the libraries and some of the functions the designer has to select the synthesis tool before he/she attempts to model the circuit at hand. Selecting the synthesis tool at the early stages leads to the selection of the libraries and so the code becomes tool specific and non portable.

In order to allow the designer the ability to use either simulators a great deal of effort went in creating multiple copies of the libraries that are compiled properly under the different simulators. Two major directories were created one for VSS and another for MTI. Under the VSS directory both SYNOVATION related packages and Synopsys related packages were both compiled using the Synopsys analyzer (VHDLAN). Under the MTI directory both SYNOVATION related packages and Synopsys related packages were both compiled using the MTI. This directory structure is shown in the following figure.

Figure 1 Directory Structure For multi-tool



Each designer created the proper initialization files for both MTI and VSS. If a designer was using SYNOVATION he/she would point to MTI/SYNOVATION and VSS/SYNOVATION. By simply recompiling the design with the proper tool either tool can be used for simulation. The ability to move from one tool to the other created a more flexible environment that we can benefit

from the strength of both tools.

5. Conclusion

VHDL is becoming the standard language for both synthesis and simulation. A single tool does not include all the features and designers have to rely on a multi-tool environment. The state of simulation and synthesis tools today leaves a lot to be desired. More standards are needed and vendors have to adhere strictly to these standards. Only then VHDL will provide portability and tool independence.

6. References:

- [1] "VSS Expert Software Tools Manual" Version 3.3a. Synopsys.
- [2] "V-System/Workstation User's Manual" Version 4. Model Technology.
- [3] "ATTSIM Multi-level Mixed-Signal Simulator. User's Guide". AT&T Design Automation.
- [4] "SYNOVATION User's Guide" AT&T Design Automation.
- [5] "Design Analyzer Reference Manual". Version 3.3a. Synopsys.