

## **A VHDL-based topdown design technique for control-dominated system: BLACKJACK**

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### **Summary**

BLACKJACK is a VHDL-based topdown design technique for control-dominated systems. The control-dominated system is a system which has complex execution thread but seldom performs arithmetic operations. It usually consists of many parts which operate in parallel and interact with each other. The technique consists of (1) design capture with a specific, behavioral style (BLACKJACK style) VHDL and (2) a conversion program (FISGEN) that builds a finite state machine with datapath (FSMD). The resulting FSMD is described in the behavioral style VHDL that can be fed into a logic synthesis tool. One process in the FISGEN input turns into one process in the FISGEN output. In the BLACKJACK style, behavior is described with "standard" programming language construct. In addition, elapse of time is explicitly specified with VHDL statement, WAIT FOR 0 ns, that introduces one delta delay. There is no restriction concerning where it is placed. The BLACKJACK style uses a simple, uniform way of modeling interprocess signal sourced by more than one process and thus can model a design which has many parts that are active simultaneously and interact with each other. Resolved signal of bit type with an appropriate resolution function and assignment to NULL model this type of signal. Bus or register kind is used depending on whether the signal is sensed only when its driver is active or it may be sensed even when the driver is not active. The modeling is done at the level where no concept of state or state transition is introduced. The captured design is simulated with a VHDL simulator and verified. There will be no advance in time in terms of second but only in terms of delta. FISGEN traverses the flow graph of the input description, introducing state transition when no more operations are possible in the state under consideration, or when a WAIT statement is encountered. The decision about no more possible operations is based on very simple criteria that are considered adequate for the targeted application domain. Interprocess communication is converted into description from which a logic synthesizer generates register/FF with multiplexors or bus driven by 3-state buffers, depending on whether register kind or bus kind is specified. The technique was tried on several control-dominated systems, including the PCI bus controller.