

VHDL MODELING GUIDELINES FOR DID COMPLIANCE (DI-EGDS-80811)

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ABSTRACT

Downsizing in the Department of Defense (DoD) and reductions in DoD funding place special emphasis on extending the life cycles of existing equipment and instituting "on demand" rapid manufacturing practices. These objectives necessitate the development of new engineering methods which address obsolescence issues and tightly couple the design and manufacturing interface. To this end, the Standard Hardware Acquisition and Reliability Program (SHARP) office sponsored the Technology Independent Representation of Electronic Products (TIREP) project to investigate VHDL circuit card assembly (CCA) modeling approaches which serve to drive a manufacturing interface. Compliance with the government VHDL Data Item Description (DID, DI-EGDS-80811) and applicability to high level design techniques were the primary criteria imposed upon the TIREP VHDL models. The DID is one provision which may be appended to government contracts to stipulate the format and content of VHDL models of delivered systems, subsystems, and components such as gate arrays and application specific integrated circuits (ASICs). The TIREP CCA VHDL models employ familiar industry standards such as the Multi-value Logic System for VHDL Model Interoperability (IEEE-STD-1164), the Waveform and Vector Exchange Specification (WAVES, IEEE-STD-1029.1) and the Commercial Component Model Specification (EIA 567/A). This paper presents the results of the TIREP VHDL

modeling effort and offers guidelines for the development of component and CCA VHDL models which are compliant with the government VHDL DID. Modeling issues not explicitly addressed by either the DID or EIA 567/A are presented and a modified EIA 567 approach which minimizes code redundancy with hierarchical CCA VHDL models is also discussed. The impact of the more recent EIA 567A specification on DID-compliant VHDL modeling is reviewed. The paper also presents one VHDL coding approach to capturing Printed Circuit Board (PCB) form factors and layout directives required by a rapid acquisition manufacturing interface.

INTRODUCTION

One of the major goals of the TIREP project is to investigate and develop a method of documenting electronic circuit card assemblies (CCAs) that contain obsolete parts. This documentation would also serve to drive the manufacturing interface for technology insertion of the new CCA. In addition to using VHDL to model the CCAs, the TIREP team decided to implement other industry standards in the models in order to ensure interoperability between models and different toolsets, to offer a more standardized approach to interfacing with manufacturing sites, and to promote future useability of the documentation of the CCAs. The team elected to make use of the example of the EIA-567 modeling approach that was developed by Mr. Len Feingold for

the U.S. Air Force's F-22 program, since it was an excellent example of a Data Item Description (DID) compliant VHDL model and adopted most of the standards we desired to use, including the Multi-value Logic System for VHDL Model Interoperability (IEEE-STD-1164), and the Commercial Component Model Specification (EIA-5670000).

Because the TIREP project is entirely a DoD sponsored effort the VHDL models that were developed were required to comply with the DID. A Data Item Description (DID) is a document which specifies the format and content instructions for a required data product. It is typically appended to a government contract to ensure that data product deliverables conform to an accepted standard and that all necessary information to support the deliverable(s) has been delivered. Capturing design data in standard formats is especially important in the case of electronic military equipment with life-cycles far in excess of similar commercial products and technologies. The VHDL DID, DI-EGDS-80811, may be appended to a contract which requires the description(s) of an electronic system, subsystem or component.

As members of the TIREP group independently modeled the electronic circuits each member had been assigned, issues with various methodologies were raised and discussed. As a result, changes were made in the methodology used that reflected an improved method of VHDL modeling for interfacing with manufacturing facilities. Among these changes was the addition of a testbench written using the Waveform and Vector Exchange Specification (WAVES) standard (IEEE-Std 1029.1).

As a result of their experience, the TIREP group decided to compile a VHDL Modeling Guide which represents the results of this VHDL modeling effort. This modeling guide offers guidelines for the development of component and CCA VHDL models which are compliant with the government DID as well as the industry standards listed above. The remainder of this paper will describe the contents of "A VHDL Modeling Guide" and address some of the modeling issues that were encountered.

MODELING GUIDE OVERVIEW

The intent of "A VHDL Modeling Guide" is not to impose requirements on the engineer, nor is it to be used as a textbook. The intent is, however, to suggest a format that if adopted by enough VHDL modelers will facilitate rapid acquisition manufacturing of replacement electronic designs resulting from obsolescence of IC devices, as well as enhancing readability and transportability of models throughout the VHDL community. The intended users of the modeling guide include the engineer with a basic knowledge of VHDL and the experienced VHDL modeler. The result of using the guide will be a DID compliant, comprehensive VHDL model, that implements the available industry standards. "A VHDL Modeling Guide" is also intended to be easily referenced. The point is not for the engineer to be intimidated by this document, but for the engineer to only reference the portions that apply to their current need. The guide also includes many examples of VHDL models that illustrate the modeling techniques described.

CHAPTER 1 OVERVIEW

Chapter 1 is an introductory chapter. Included in this chapter are reference documents, definitions, and acronyms that are used throughout the modeling guide in order to remove ambiguities.

CHAPTER 2 OVERVIEW

Chapter 2 provides recommended modeling conventions. A list of suggested file naming conventions, VHDL design unit naming conventions, and pin and signal naming conventions are included. In the case of the TIREP group, the adoption of a consistent naming convention was very important for the manufacturing interface with the Rapid Acquisition of Manufactured Parts (RAMP) facility. This facility, located at NAWC, Indianapolis, is the manufacturing site of the redesigned CCAs developed by the TIREP team, using VHDL, to replace the obsolete parts. The RAMP facility developed an interface for the first VHDL model TIREP

submitted to them for manufacture, using the naming conventions that are described in "A VHDL Modeling Guide". Then, for the remanufacture of subsequent designs, if the VHDL models of these designs implement the same naming conventions, the interface that was developed for the first design can be reused at the manufacturing site and the manufacturing process becomes more automated, more efficient, and less costly. An example of some of the naming conventions described in the modeling guide are:

<filename>.<extension> where extensions shall be as follows

Extension	File Type/Description
.vhd	A VHDL source file
.wav	A VHDL WAVES source file

Design Abstraction	Architecture Name
behavioral	arch_<design_name>_beh
structural	arch_<design_name>_str

This chapter also provides the structure and content of the files used in the TIREP models and indicates whether or not changes need to be made to adapt these files to another design. (This is described in detail in Chapter 3). Figure 1 illustrates the VHDL model structure used for the TIREP models.

This chapter also includes reference lists of: predefined VHDL data types; predefined VHDL operators; and lists of reserved words for VHDL 1076, the VHDL Standard Package, the VHDL TEXTIO Package, WAVES, the multi-value logic (IEEE-STD 1164) package, and EIA-567 packages.

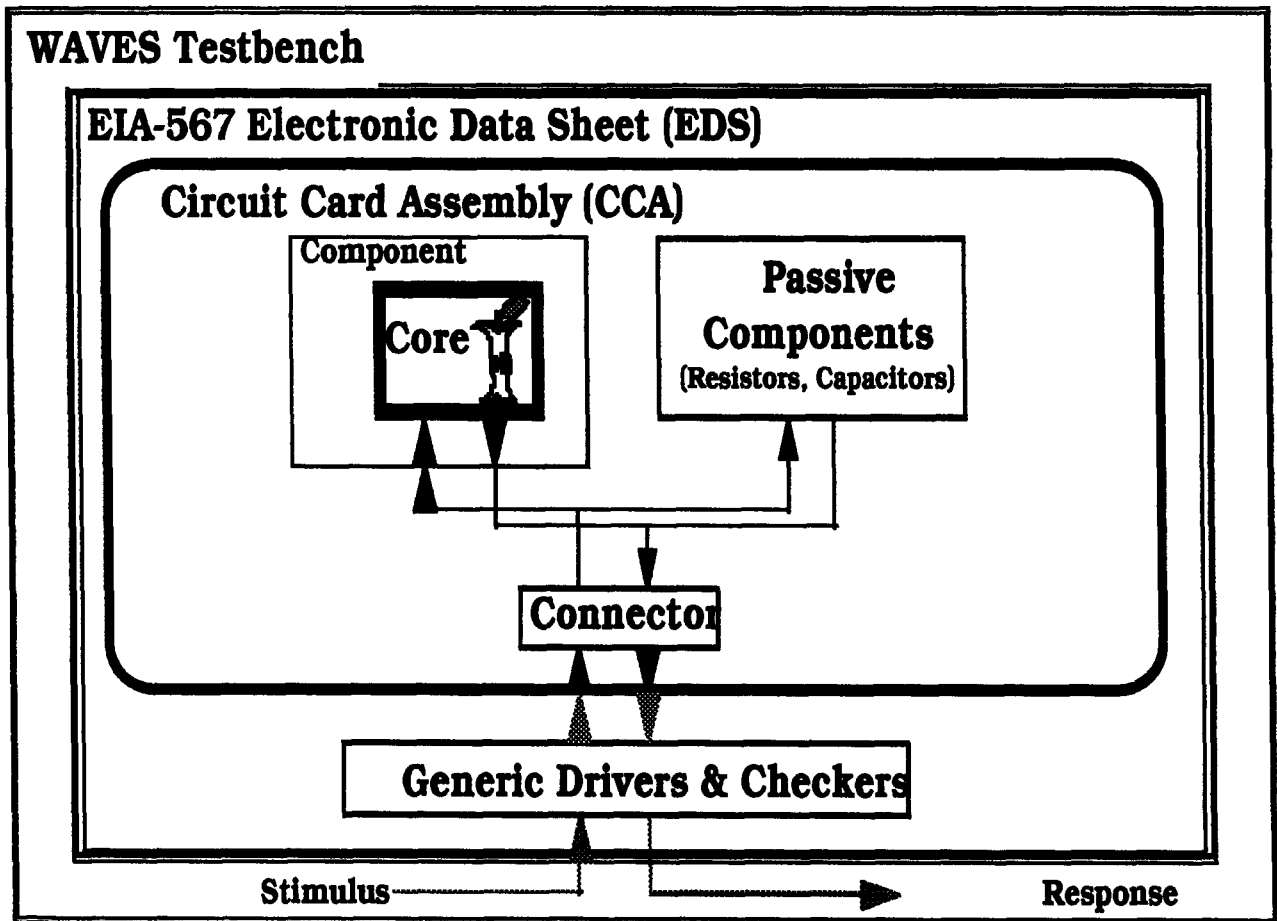


Figure 1. The TIREP VHDL Model Structure

CHAPTER 3 OVERVIEW

This chapter was established to provide a template approach to the development of a DID compliant VHDL model. It is hoped that this chapter will give the design engineer a "quick start" entry into model development. In this chapter, the design engineer is given a list of the files that will support their model without any changes, along with references to the chapters that explain the files in depth. Using an example model of a CD4029B counter and data of the static and dynamic electrical characteristics taken directly from the data sheet of the CD4029B, the engineer is then walked through each file that would require changes to support their model all the way through the WAVES testbench, and told where to insert the information that is applicable to their design. This example includes extensive comments explaining the information that is required within the model. The types and constants that are declared in the model are also defined in a hardware sense.

CHAPTER 4 OVERVIEW

In chapter 4 the modeling approach defined by Mr. Len Feingold, which is based on the EIA-567 Commercial Component Specification, is presented and discussed. Instead of using the Viterbi decoder model Mr. Feingold developed for the Air Force's F-22 project, one of the TIREP models is used as an example. In accordance with the SHARP program, the TIREP models represent the efforts of the TIREP group in addressing real obsolescence problems of in-service Navy combat systems. The model is of an 'A' size Standard Electronic Module (SEM) with key code FBG, which is a population counter. This module is used in the AN/SQS-53 SONAR System, which was integrated into the AN/SQQ-89 Combat ASW System back in the late 80's.

The goal of the EIA-567 modeling approach is to develop an Electronic Data Sheet (EDS) for a component, sub-assembly, assembly or system using VHDL. Elements that are modeled in the EDS include input/output pin characteristics (min/max operating currents, voltages, propagation delays and loads), timing constraints (such as setup and

hold times and/or min/max pulse widths), and operating point conditions (such as voltage, power, temperature, package type, radiation hardness, etc.).

Len Feingold approached the EIA-567 EDS requirements by describing a core behavioral model around which generic drivers and checkers are added to implement timing characteristics. These models are:

Component	Component Description
i_driver	Input driver
t_driver	Output driver with tri-state capability
b_driver	Bi-directional driver
sync_checker	Synchronous constraint checker (setup and hold times)
async_checker	Asynchronous constraint checker (minimum and maximum pulse widths)

These generic drivers and checkers are then supported by the EDS packages. They consist of the four EIA-567 packages and three design packages listed below.

Package	Package Description
eia_567_ev	Electrical view package Establishes the data types to define port characteristics
<design>_ev	Electrical view package Defines the port characteristics for the design
eia_567_tv	Timing view package Establishes the data types to define port timing
<design>_tv	Timing view package Defines the port timing for the design
eia_567_pv	Physical view package Establishes the data types which define the electronic data sheet
<design>_pv	Physical view package Define the electronic data sheet
eia_567_tb	Toolbox package Defines functions used in support of the electronic data sheet

During the discussion of these models, advantages and disadvantages of Mr.

Feingold's modeling approach are presented in the modeling guide.

CHAPTER 5 OVERVIEW

This chapter was established to address some of the concerns and limitations the TIREP team found in the EIA-567 modeling approach described in Chapter 4. In the interest of not re-writing Chapter 5 of the VHDL modeling guide, this paper will simply list a few of the issues that were raised as an example, and will leave it up to the reader to reference the modeling guide for further explanation.

The output driver components used to model propagation delays do not take into consideration transition time modeling. The "eia_567_tv" package was expanded to include transition times in the definition of type delay. The TIREP output driver model warns the user if a transition time is specified that is greater than two times the specified propagation delay.

The relationship of the electrical view class in the "design_ev" file to the pins on the model is inferred, not explicit. This link is completed by adding a generic clause to the driver components. At the present state of the TIREP model development, the added generic link provides no functional benefit. The explicit link was developed for future use of the model in the area of test and evaluation of hardware.

The EIA-567 electrical view package employs the use of "classes" to define load circuits to be applied to a model. While this provides a viable approach to the documentation of these circuits, it is limited by the fact that it will not support machine interpretation of the circuit unless a standard load configuration is adopted. For the purpose of the modeling guide, the "load class" approach identified through the EIA-567 packages has been adopted for the time being. Additional investigation is being performed to determine if a more standardized approach is in order.

The output of the input driver model described in Chapter 4 is limited to the XO1 subtype. This has positive and negative ramifications. On one hand, it can use the

RISING_EDGE and FALLING_EDGE functions from the STD_LOGIC_1164 package which only work for '1' to '0' and '0' to '1' transitions. However, this feature restricts the STD_LOGIC state which can be used by the model. Tri-state outputs cannot be implemented as part of the behavior of the core model, but have to be implemented in the output driver instead.

A major realignment of the eia_567 packages and the <design>_eia_567 packages was done in the effort to reduce the number of files required by a design. In the method described in Chapter 4, only the eia_567_ev package could be placed in a library and used by other design units. All other packages, the generic drivers, and checkers had to be analyzed for each model due to the placement of functions upon which these components are dependent. Part of Chapter 5 describes the approach that was taken to maximize the number of general purpose functions and components which can be placed in a library which would minimize the amount of duplicate code. This consolidated version of the modeling hierarchy is also the version that is demonstrated in Chapter 3 of the modeling guide in the template. The resultant hierarchy of VHDL models in the TIREP model file structure (excluding the WAVES testbench) is:

Component /Package	Component /Package Description
<component>_core	Behavioral/Synthesizable core model of design
<component>_comp	Component models associated with design
i_driver	Input driver
o_driver	Output driver
b_driver	Bi-directional driver
async_checker	Asynchronous constraint checker (min/max pulse widths)
sync_checker	Synchronous constraint checker (setup and hold times)
eia_567	Global EIA-567 library
eia_567_ds	Design specific EIA-567 definitions
<design>_ds	Design specific package
<design>_eds	Electronic Data Sheet

The VHDL model example presented in chapter 5 is of a DQD SEM, which is another TIREP model. The author of this model presents a VHDL coding approach to capturing Printed Circuit Board (PCB) form factors and layout directives required by the RAMP facility. A brief description of these models that are discussed follows:

Component	Description
part	A generic part component for components with no electrical function (eg. mechanical)
capacitor	A capacitor component for use in a structural VHDL model of a circuit card assembly
resistor_network	A resistor network component for use in a structural VHDL model of a circuit card assembly.
graphic	A graphics package which contains definitions necessary to describe a physical entity (such as a printed wiring board form factor).
design_pcb	Provides the basic requirements for the design's printed wiring board. Contains attached generics that provide the pcb form factor along with routing restrictions and requirements
connector	Several methods of modeling connectors are presented (ie. input, output, input/output).

It should be noted that the "design_pcb" model is an approximate model. The TIREP team is currently investigating other methods of describing a physical entity such as form factor, routing restrictions, etc. that may be more easily interfaced with a manufacturing facility.

The author finally ties the components, parts, capacitors, resistors, and connectors together into a structural Circuit Card Assembly of the DQD model.

CHAPTER 6 OVERVIEW

This chapter is intended to introduce an engineer to the Waveform and Vector Exchange Specification. The WAVES Standard Packages are broken down and their respective type, subtype, and package definitions are listed to help the engineer understand the relationships between them. A copy of these standard packages is also provided.

The VHDL Modeling Guide uses a WAVES test bench of the DQD SEM to illustrate the use of design specific WAVES files as it describes the different functions and data types involved.

CONCLUSION

The TIREP group has developed a methodology of documenting electronic circuit card assemblies to facilitate rapid redesign and remanufacture of CCAs containing obsolete parts. This methodology adheres to government imposed requirements (ie. DI-EGDS-80811) and many lessons have been learned along the way. "A VHDL Modeling Guide" was compiled by the TIREP group to share those lessons learned with others. The modeling guide was intended to provide some direction to the efforts of VHDL modelers in writing DID compliant VHDL models that also make use of other industry standards that are available. The purpose of this paper was not to describe each individual issue that was addressed by the TIREP team, but to introduce "A VHDL Modeling Guide" to VHDL modelers in which the efforts of the TIREP team are discussed and VHDL examples are provided which illustrate the solutions.

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