

A Hybrid Design Methodology of LSIs and Multichip Module using VHDL

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Abstract

This presentation describes a hybrid design methodology of LSIs and MCM (Multichip Module) using VHDL as an example of NEC's experiences.

This hybrid design methodology applies VHDL design methods only to function level design, and traditional design methods to gate level design. LSIs which are mentioned here are custom LSIs, and timing and function libraries for VHDL simulator are not supported yet. Further, it is very difficult to synthesize their gate level circuits, because high performances are required at about 200MHz clock. Using this hybrid design method, these LSIs on MCM were developed in a short period.

Three kinds of LSI and MCM were developed using VHDL concurrently. MCM is composed of 3 kinds of LSIs, 14 LSIs in total. LSIs are described as behavioral VHDL model, and a VHDL structural model of MCM corresponds to more than 1300K gates level circuits.

This presentation will highlight our CAD environment and experiences to develop these LSIs and MCM.

In conclusion, we will show our plan for developing methodologies using VHDL and requirements for EDA vendor.

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Outline

1) Hybrid design methodology

For developing LSI and Multichip Module (MCM)

- An example of NEC's experiences

2) Requests for EDA vendors

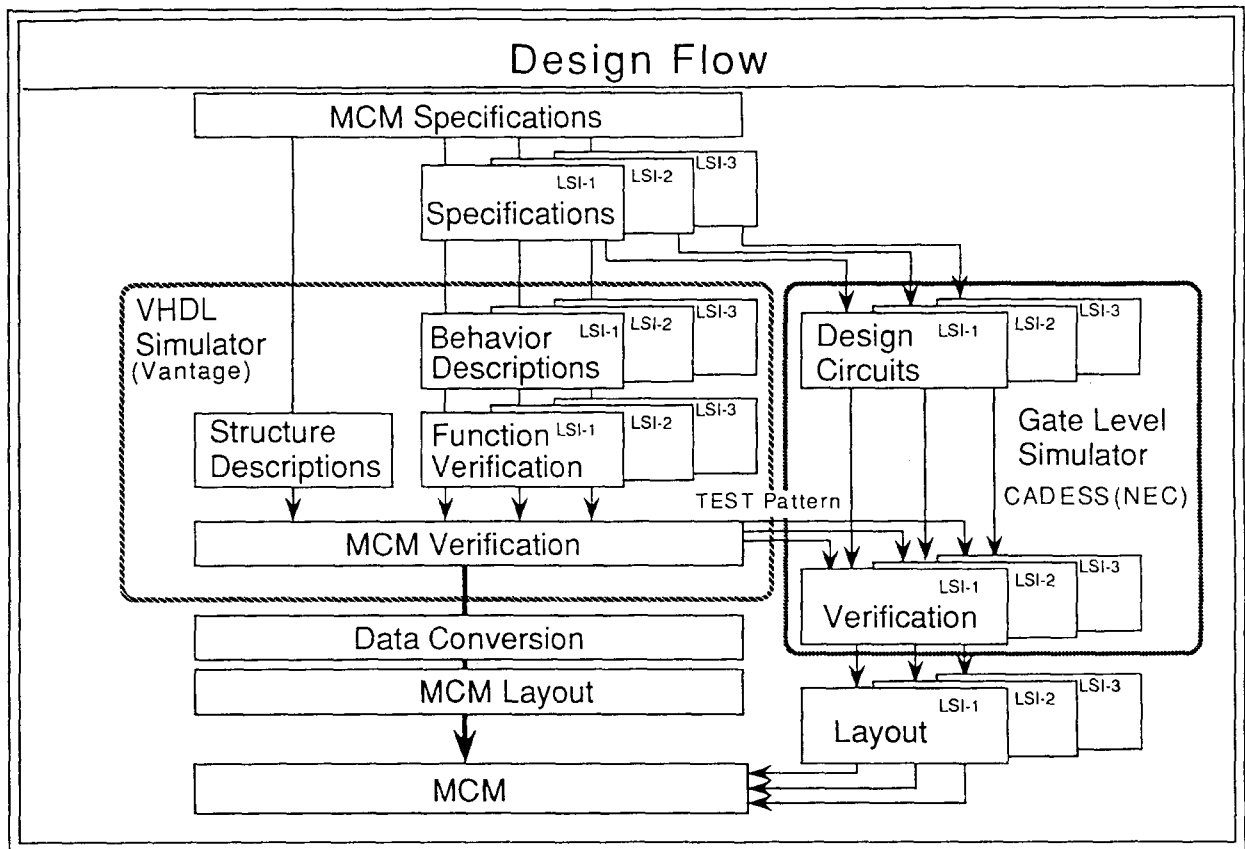
Hybrid Design Methodology

- 1) Design methodology using both VHDL design environment and traditional design environment.
- 2) Specifications of functions and interfaces are verified in VHDL design environment.
- 3) Circuit diagrams which are designed manually and by logic synthesis tools are inspected in traditional design environment.

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Why Hybrid Design Methodology?

- 1) NEC VHDL standard libraries are not supported.
It is easy to develop our own VHDL libraries, but these libraries don't apply to all design process of NEC. It is necessary to develop NEC standard libraries, function libraries and timing libraries.
- 2) Concerning timing inspection, traditional design environment is better than VHDL design environment.(e.g. backannotation) .
- 3) Applying VHDL to upstream activities of top-down design is important.
Efficiencies can be improved by applying VHDL to behavioral level even if VHDL is not applied to RTL and gate level.



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- ### Points of Design Flow
- 1) LSI specifications were verified by VHDL behavioral model.
 - 2) Functions and timings of LSI which were designed manually were verified by traditional gate level simulator.
 - 3) The test bench generated 3 kinds of test pattern for LSI verification concurrently.
 - 4) Structure descriptions of MCM were converted by support tool.
 - 5) Structure descriptions of MCM were converted to netlists for layout tool.
 - 6) Three kinds of LSI and MCM were developed at the same time.

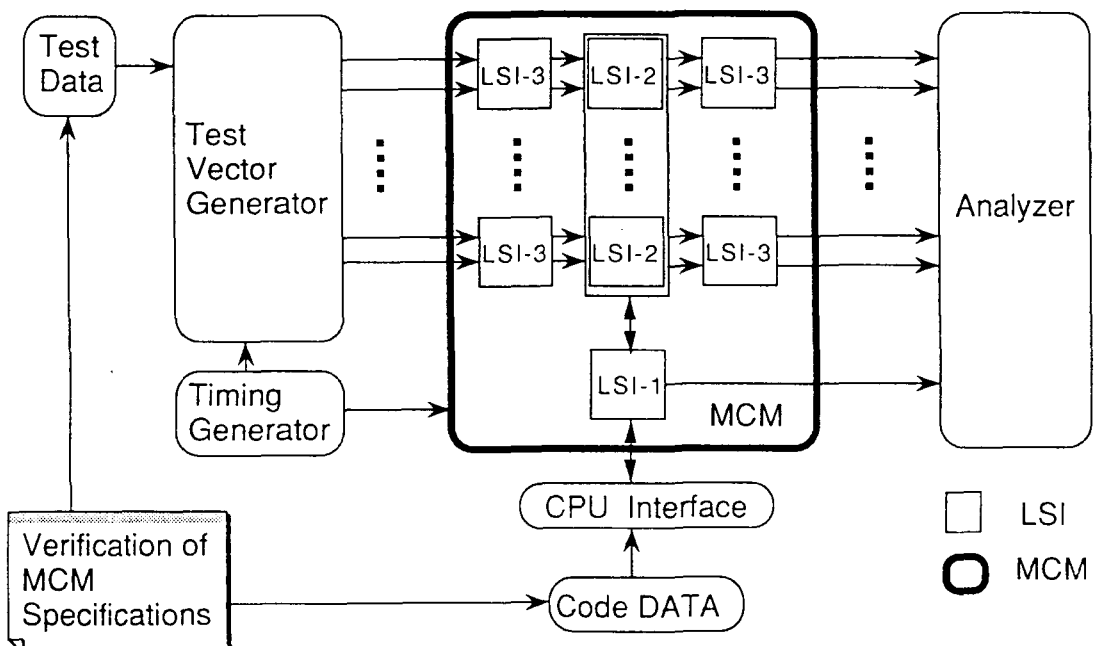
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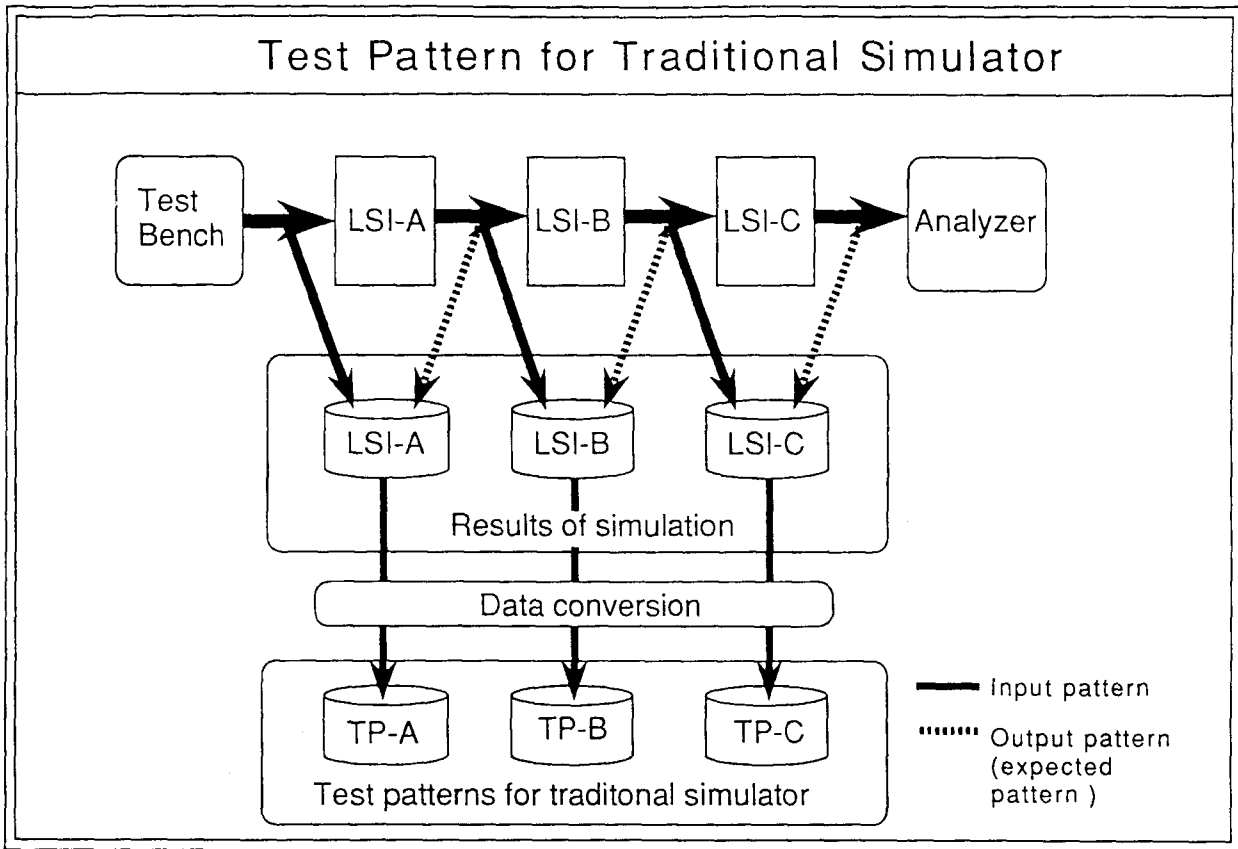
Why was not logic synthesis tool used?

- 1) VHDL gives a lot of merits to engineers even if logic synthesis is not used.
- 2) Concerning high speed circuits, VHDL description level for logic synthesis is low. These descriptions are equal to manually designed circuits. No merit to use logic synthesis tool.
- 3) VHDL libraries for custom LSI were not supported.
- 4) In circuit diagrams which are synthesized by logic synthesis tool, layout of parts is too poor to understand these circuits.
- 5) There was no engineer to have skills to use logic synthesis tool then , because engineer must get skills to use it through trial and error.

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Testbench





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Generating Test Patterns from Testbench

Easy to generate test patterns for LSI verification

Traditional design method :

Engineers spent much time to draw waveforms.

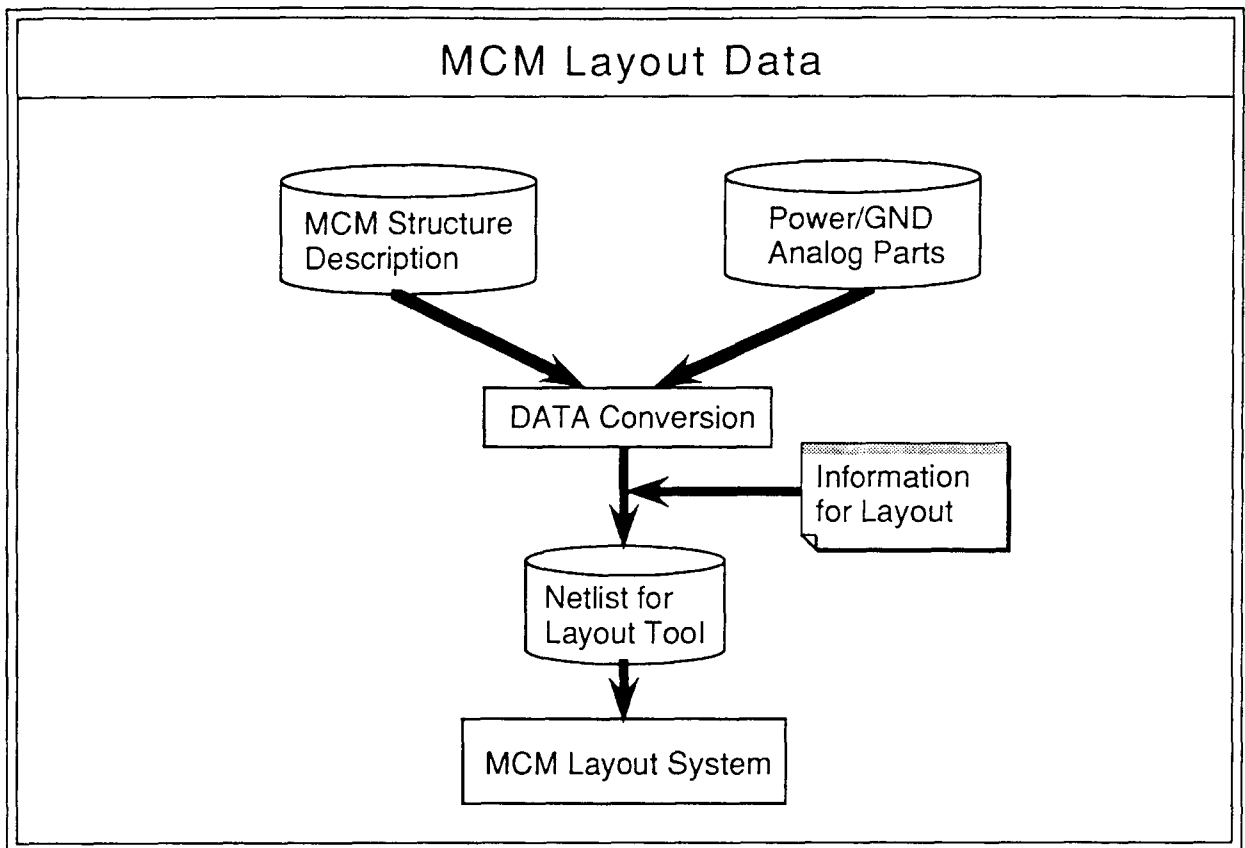
Hybrid design method :

Three kinds of LSI test pattern are generated from testbench concurrently.

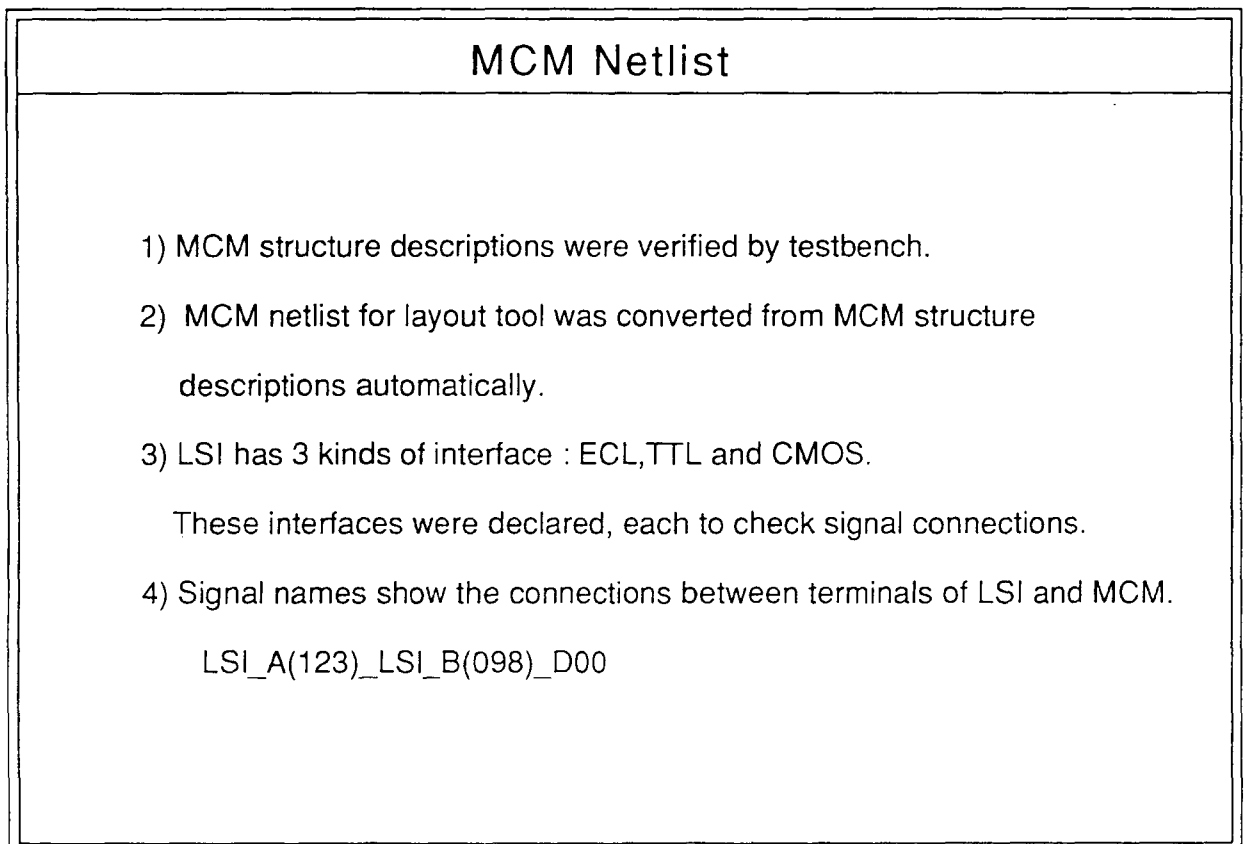
Productivity

traditional method :	1
this method :	more than 3

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Integration of LSI

	Number of Logic Gates	Memory Size
LSI-A	113K	———
LSI-B	90K	114Kbit
LSI-C	100K	43Kbit

Note)
 LSI Package : 320 pin Butt Lead
 Clock Speed : max 200 MHz

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Integration of MCM

	Number of LSI	Number of Logic Gates	Number of MCM Terminals	Number of Nets
CASE-1	9	870K	———	———
CASE-2	14	1300K	2700	1457
CASE-3	26	2500K	———	———

Note)
 1) CASE-2 : Developed MCM
 2) Clock Speed : max 200 MHz

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VHDL Source

		Number of source lines
Bench	Testbench	5459
LSI	LSI-A	3675
	LSI-B	3912
	LSI-C	5487
MCM	CASE-1	7503
	CASE-2	10008
	CASE-3	15011

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Activities of our group

- 1) Educating engineers for VHDL design (more than 100 engineers) .
- 2) Developing VHDL design environments.
 - developing VHDL libraries for simulator and logic synthesis tool.
 - developing design methodologies.
 - developing many usefull support tools.
 - improving technique to use logic synthesis tool.
- 3) Cultivating of engineer's and manager's consciousness for VHDL design.
- 4) Continuing to design LSIs with this hybrid design methodology.

Requests to EDA vendor

- 1) Developing high abstraction logic synthesis
- 2) Developing formal verification tool between behavioral model and RTL model.
- 3) Free description style
Don't force users to change VHDL description style, because user's purpose is not to use tools and users have their own description style.
- 4) Specifying limitations of tools.
(e.g. gate size,the number of signals)
- 5) Training technical support engineers in JAPAN .

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Conclusion

This presentation described a hybrid design methodology for LSI and Multichip Module(MCM) as an example of NEC's experiences. This methodology is very usefull while logic synthesis tools are still poor.

It gives good results to apply VHDL to the design of LSI, printed wiring board and MCM. It will be tried to simulate the total system including software in the near future.