

METHOD1076
VHDL based VLSI/COMPUTER design methodology

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Abstract

This paper describes VLSI design experience and new design challenges by VHDL in PFU

Our objects of using VHDL in order to design VLSI effectively are adaptation of top-down design/logic synthesis/system simulation methodologies and to establish new design methodology(METHOD1076) harmonized with these three methodologies ,so-called "concurrent engineering".

So we tried to use VHDL in the wide range of design processes.

Generally,many reported VHDL uses has been seen at just behavioral stage, however our approach includes functional design,logic synthesis,gate level design, library representation and test bench expressions.

As concrete trials,we did followings for real-product-level computer development.

- 1. VHDL Package/CMOS Library development**
- 2. Tool integration**
- 3. Logic synthesis from VHDL**
- 4. VHDL mixed model system simulation**
- 5. VHDL multi level system simulation**
- 6. VHDL full-timing delay simulation**

And through our experience,we also comment for

- 1. VHDL adaption process,designer training**
- 2. VHDL issues**

Finally,PFU claims following conclusions through two years VHDL design experiences.

"VHDL is fully able to be used for IC design and computer system design"

"VHDL is design methodology and comprehensive design environment "

VHDL INTERNATIONAL USER'S FORUM 92 FALL

METHOD 1076
VHDL(IEEE1076-1987) BASED DESIGN

Wednesday, OCT21

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- New design Methodology
- VHDL design status
- Design style
- VHDL design issues
- Conclusion

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NEW Computer Design Methodology based upon VHDL

1. Top-Down Design/Functional Verification

Higher abstraction level for design and verification

2. Logic Synthesis

Driving design automation / Schematic->Description language

3. System Simulation

Simulation area expansion / Chip->System

Hermonize three Methodologies to
realize CONCURRENT ENGINEERING

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VHDL Utilization

Establish single simulator environment by VHDL simulator
Establish IC/CAD vendor independent design environment

	OLD		NEW
<input type="checkbox"/> Behavioral expression	CAD VENDOR FORMAT	→	VHDL
<input type="checkbox"/> Synthesis expression	CAD VENDOR FORMAT	→	VHDL
<input type="checkbox"/> Netlist expression	IC VENDOR FORMAT	→	VHDL
<input type="checkbox"/> Library expression	IC VENDOR FORMAT	→	VHDL
<input type="checkbox"/> Test bench	IC VENDOR FORMAT	→	VHDL

Vendor Independent Design Data Management
Selection of most advanced technology among IC vendors
Flexible CAD vendor Selection

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VHDL Design Status

- Create PFU original VHDL package
- Create Fujitsu CMOS VHDL library
- Tool integration using VHDL interface
VHDL simulator/VHDL synthesizer/Schematic Capture
- Design VLSI Chips using Logic Synthesis
- Realizing VHDL mixed model system simulation
VHDL model/SmartModel/Realchip model
- Realizing VHDL multi level system simulation
Behavioral/RTL/Gate level
- Realizing VHDL full-timing simulation

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Package/Library Development

Original Package/Library Development

- PFU original VHDL Package
Multi value Definition/Create over loading functions
- Functional Fujitsu/CMOS Cell Library
for Multi level simulation
- Full-timing Fujitsu CMOS Cell Library
(includes Delay calculation/Back annotation)
for full-timing delay simulation

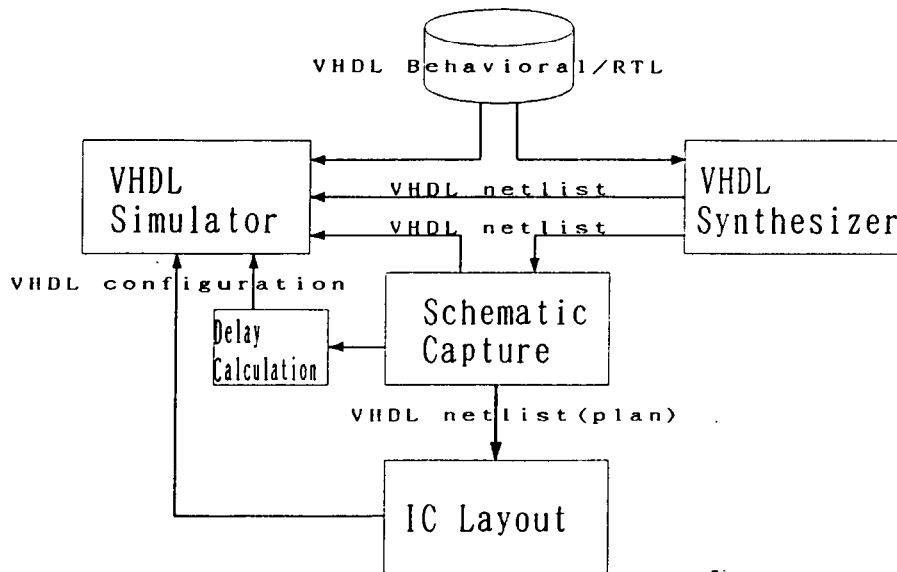
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Tool Integration

Integrate VHDL Tools by pure VHDL interface



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VHDL Design Chips

1. ASIC1 3,000 gates/CMOS
100% VHDL design
Tried multi vendor implementation
2. ASIC2 40,000 gates/CMOS
50% existing design
50% VHDL design
3. ASIC3 250,000 gates/CMOS
100% VHDL design

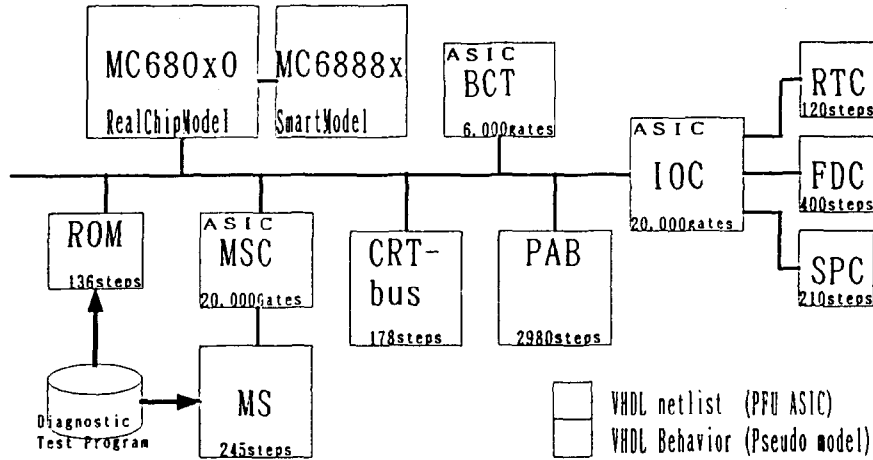
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VHDL Mixed model system simulation

Workstation CPU board simulation



Mixed model (RealChip, SmartModel, VHDL model) simulation on VHDL simulator

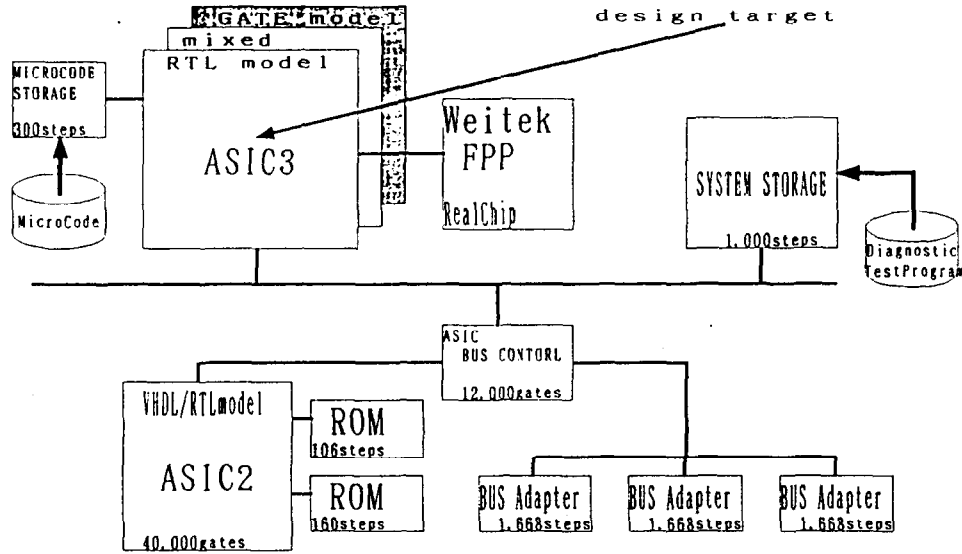
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VHDL multi level system simulation

Business host computer CPU board simulation



Multi level (Behavioral/RTL/Gate level) Design for ASIC3

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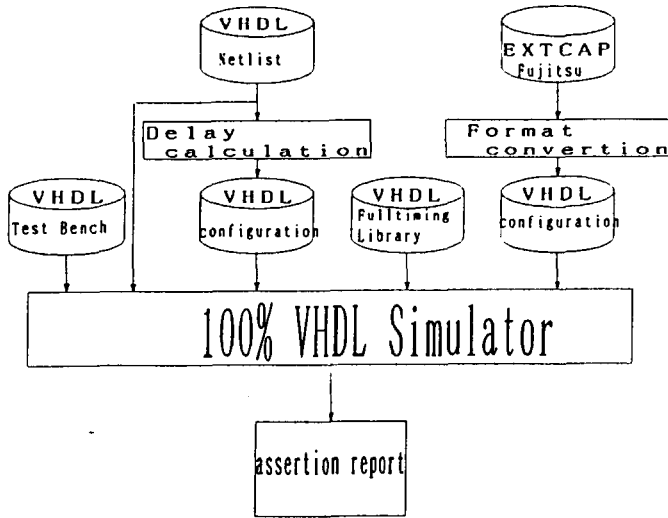
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VHDL Full-timing delay simulation

PFU Full-timing simulation flow

Forward annotation Back annotation



Benchmark report

40,000gate/1000vector pattern

SPARCSTATION2/64MB

simulation time

VANTAGE4.0 Timing

VANTAGE4.0 function

VERILOG-XL Timing

To be announced hopefully

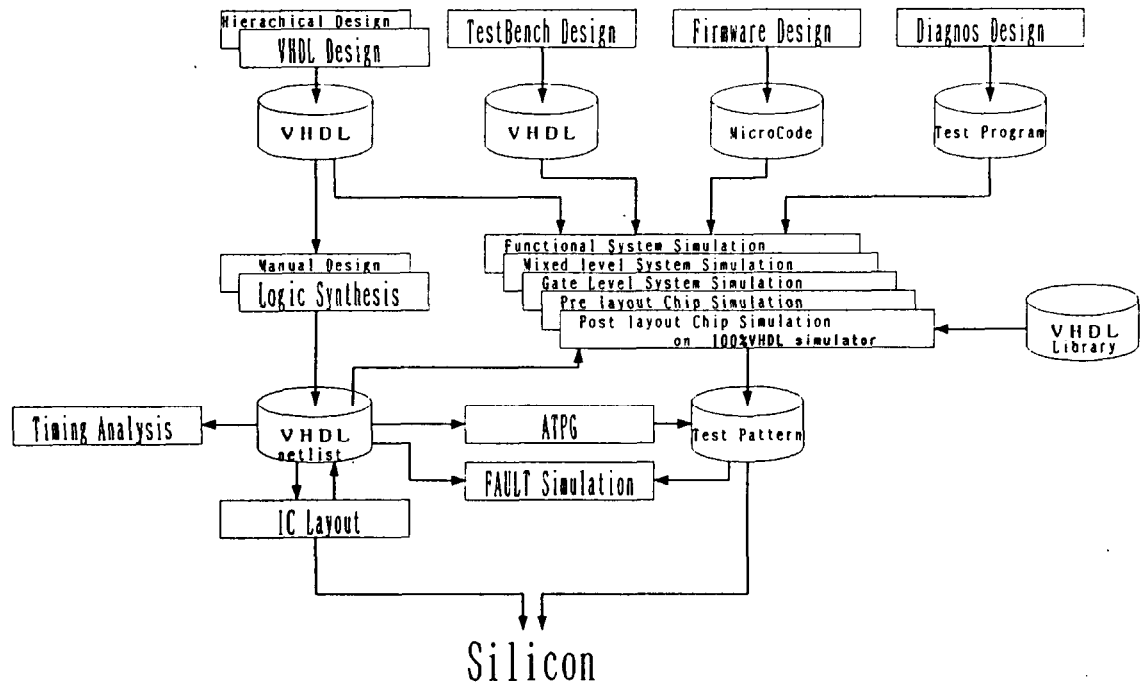
LCADFE
FUJITSU Timing

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Design Flow

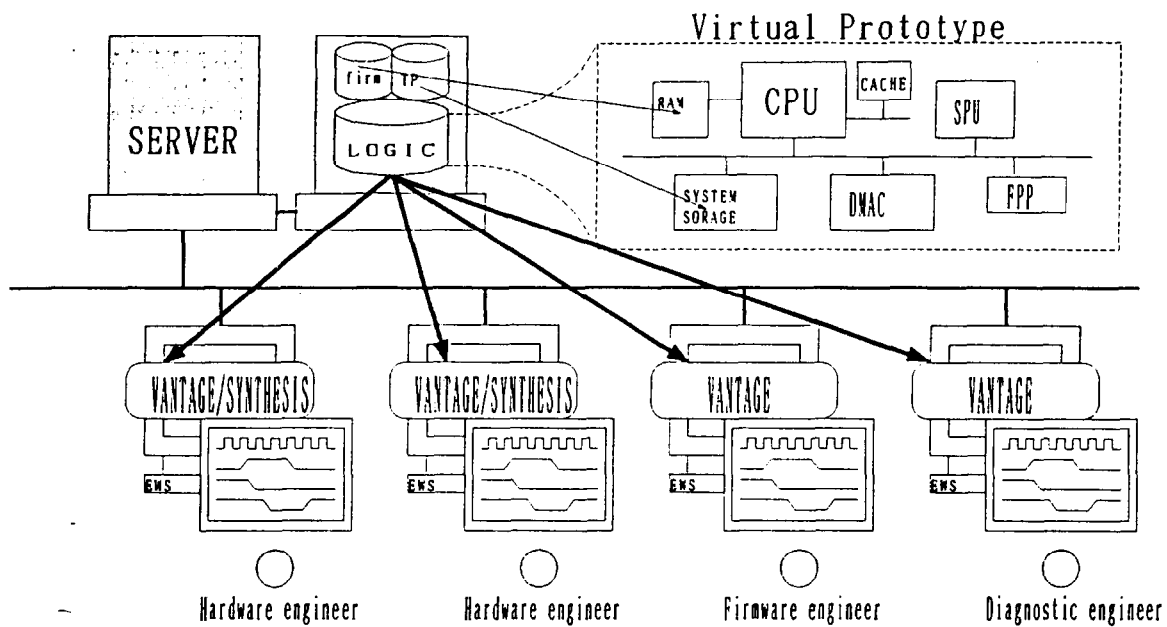


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Design style in System Simulation



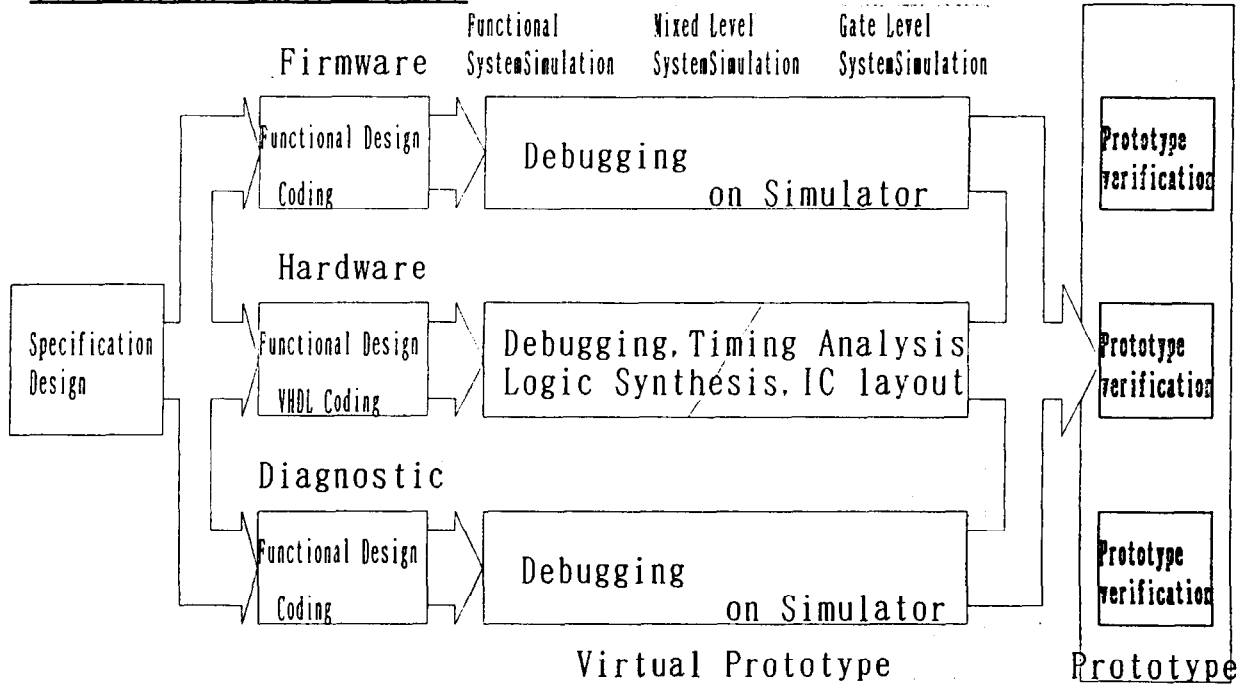
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METHOD 1076 CONCURRENT ENGINEERING I

← Early System verification

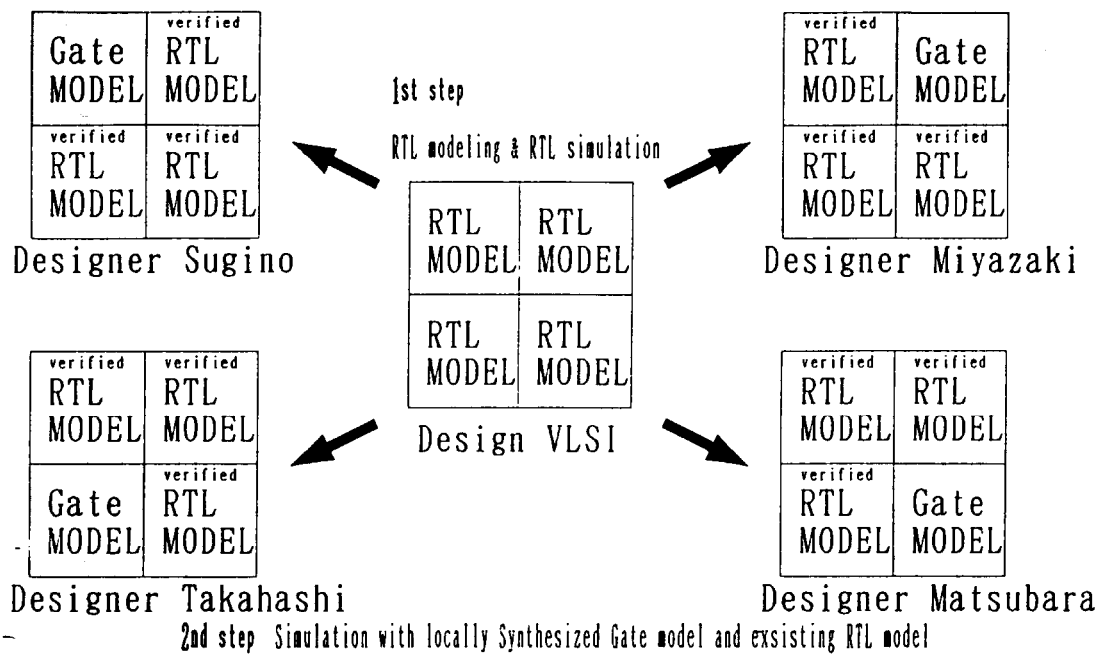


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METHOD 1076 CONCURRENT ENGINEERING2



Simulation performance & design process improving!!

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VHDL Design Issues

VHDL user should overcome several issues

- Coding Style decision for reviewing/design data exchange
- Differences of VHDL support level (simulator VS synthesizer)
- VHDL netlist output from Schematic (reflection of BUS & ripper expression)
- VHDL netlist -> Schematic Capture (Schematic attribute)
- VHDL netlist <-> Inhouse-netlist (configuration information)
- Capital distinction (VHDL simulator VS other CAE tools)
- Multi architecture design data management (VHDL source code)
- Multi architecture design data management (library in other tools)
- X propagation handling in RTL model

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User necessities for VHDL

- IC vendor should release VHDL Packages for Sign-off VHDL Simulation
- VHDL TTL standard models
- Standard style of back annotation mechanism
- Common VHDL library control among Simulator, Schematics, Synthesis, and Other tools
- Standard guideline of VHDL netlist
- Standard conversion style between EDIF and VHDL netlist

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Conclusion

VHDL is fully able to be used for VLSI/computer design.

VHDL is design methodology & design environment.

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