METHOD1076
VHDL based VLSI/COMPUTER design methodology

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Abstract

This paper describes VLSI design experience and new design challenges by VHDL in PFU

Our objects of using VHDL in order to design VLSI effectively are adaptation of
top-down design/logic synthesis/system simulation methodologies and to establish
new design methodology(METHOD1076) harmonized with these three methodologies
,so-called "concurrent engineering".
So we tried to use VHDL in the wide range of design processes.
Generally,many reported VHDL uses has been seen at just behavioral stage,
however our approach includes functional design,logic synthesis,gate level design,
library representation and test bench expressions.
As concrete trials,we did followings for real-product-level computer development.

1. VHDL Package/CMOS Library development
2. Tool Integration
3. Logic synthesis from VHDL
4. VHDL mixed model system simulation
5. VHDL multi level system simulation
6. VHDL full-timing delay simulation

And through our experience,we also comment for

1. VHDL adaption process,designer training
2. VHDL issues

Finally,PFU claims following conclusions through two years VHDL design experiences.

"VHDL is fully able to be used for IC design and computer system design"

"VHDL is design methodology and comprehensive design environment"
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□ New design Methodology
□ VHDL design status
□ Design style
□ VHDL design issues
□ Conclusion
NEW Computer Design Methodology based upon VHDL

1. Top-Down Design/Functional Verification
   Higher abstraction level for design and verification

2. Logic Synthesis
   Driving design automation/Schematic->Description language

3. System Simulation
   Simulation area expansion/Chip->System

Hermonize three Methodologies to realize CONCURRENT ENGINEERING

VHDL Utilization

Establish single simulator environment by VHDL simulator
Establish IC/CAD vendor independent design environment

OLD

- Behavioral expression
- Synthesis expression
- Netlist expression
- Library expression
- Test bench

NEW

- CAD VENDOR FORMAT ➔ VHDL
- CAD VENDOR FORMAT ➔ VHDL
- IC VENDOR FORMAT ➔ VHDL
- IC VENDOR FORMAT ➔ VHDL
- IC VENDOR FORMAT ➔ VHDL

Vendor Independent Design Data Management
Selection of most advanced technology among IC vendors
Flexible CAD vendor Selection
**VHDL Design Status**

- Create PFU original VHDL package
- Create Fujitsu CMOS VHDL library
- Tool integration using VHDL interface
  VHDL simulator/VHDL synthesizer/Schematic Capture
- Design VLSI Chips using Logic Synthesis
- Realizing VHDL mixed model system simulation
  VHDL model/SmartModel/Realchip model
- Realizing VHDL multi level system simulation
  Behavioral/RTL/Gate level
- Realizing VHDL full-timing simulation

**Package/Library Development**

Original Package/Library Development

- PFU original VHDL Package
  Multi value Definition/Create over loading functions
- Functional Fujitsu/CMOS Cell Library
  for Multi level simulation
- Full-timing Fujitsu CMOS Cell Library
  (includes Delay calculation/Back annotation)
  for full-timing delay simulation
Tool Integration

Integrate VHDL Tools by pure VHDL interface

VHDL Behavioral/RTL

VHDL Simulator

VHDL netlist

VHDL Synthesizer

VHDL netlist

VHDL configuration

Schematic Capture

Delay Calculation

VHDL netlist (plan)

IC Layout

VHDL Design Chips

1. ASIC1 3,000 gates/CMOS

100% VHDL design
Tried multi vendor implementation

2. ASIC2 40,000 gates/CMOS

50% existing design
50% VHDL design

3. ASIC3 250,000 gates/CMOS

100% VHDL design

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METHOD 1076
VHDL (IEEE 1076-1987) BASED DESIGN
**VHDL Mixed model system simulation**

Workstation CPU board simulation

- **MC680x0** RealChip Model
- **MC6888x** SmartModel
- **ASIC RCT** 6,000 gates
- **RTC** 10,000 gates
- **ASIC IOC** 20,000 gates
- **FDC** 40,000 gates
- **SPC** 20,000 gates

Mixed model (RealChip, SmartModel, VHDL model) simulation on VHDL simulator

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**VHDL multi level system simulation**

Business host computer CPU board simulation

- **MICROCODE STORAGE** 10,000 gates
- **MicroCode**
- **RTL model**
- **ASIC3**
- **ASICE FPP** RealChip
- **SYSTEM STORAGE** 1,000 gates
- **ASIC BUS CONTROL** 1,000 gates
- **ROM** 10,000 gates
- **ROM** 10,000 gates
- **ROM** 10,000 gates
- **BUS Adapter** 1,000 gates
- **BUS Adapter** 1,000 gates
- **BUS Adapter** 1,000 gates

Multi level (Behavioral/RTL/Gate level) Design for ASIC3

1992 FALL written by H. SHINE 9
**VHDL Design Issues**

VHDL user should overcome several issues

- **Coding Style**: decision for reviewing/design data exchange
- **Differences of VHDL support level**: (simulator VS synthesizer)
- **VHDL netlist output from Schematic**: (reflection of BUS & ripper expression)
- **VHDL netlist -> Schematic Capture**: (Schematic attribute)
- **VHDL netlist <-> Inhouse-netlist**: (configuration information)
- **Capital distinction**: (VHDL simulator VS other CAD tools)
- **Multi architecture design data management**: (VHDL source code)
- **Multi architecture design data management**: (library in other tools)
- **X propagation handling in RTL model**
User necessities for VHDL

- IC vendor should release VHDL Packages for Sign-off VHDL Simulation
- VHDL TTL standard models
- Standard style of back annotation mechanism
- Common VHDL library control among Simulator, Schematics, Synthesis, and Other tools
- Standard guideline of VHDL netlist
- Standard conversion style between EDIF and VHDL netlist

**Conclusion**

VHDL is fully able to be used for VLSI/computer design.

VHDL is design methodology & design environment.