

A Design Automation Tool to Generate the Schematics and VHDL Description of a Circuit by Extraction of VLSI Layout

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Abstract

A design automation tool that performs extraction on VLSI layouts to generate circuit schematic and VHDL description, is developed in this research. From a layout given in Caltech Intermediate Format, the schematic description in Electronic Design Interface Format (EDIF) is generated. The multi-level extraction process identifies various components of the circuit and prepares the necessary database to represent components and their connectivity. This database is used to generate the EDIF schematic of the circuit. The connectivity among the components is shown by writing the routing for all the signals of the circuit. The ports on each symbol of the schematic have some VHDL attributes associated with them. The VHDL attributes such as port_mode and port_type are written with EDIF cell description.

Most of the commercial VHDL environments provide a facility for importing EDIF descriptions. After importing the EDIF design description, the schematic of a circuit can be viewed or edited in the design environment. From within the design environment, the VHDL structural description for the entire circuit can be obtained by compiling the EDIF schematic file. The VHDL attributes allow simulation of the circuit at the gate level within the host environment.

Several example circuits were extracted using this tool and imported into the Vantage Spreadsheet for simulation of the design, viewing of the schematics, and generation of structural VHDL code. Being able to simulate the design at the gate level in commercial tools such as the Vantage Spreadsheet, provides significant improvement in simulation time for observation of the functional behavior of a circuit versus switch level simulation.

References:

- (1) M. Dukes, "Generalized Extraction System for VLSI", Electronic Technology Laboratory, Wright-Patterson Airforce Base, Dayton, OH. 1990. Document WRDC-TR-90-5021
- (2) ANSI/EIA-548-1988, Electronic Design Interchange Format, Version 2.0.0 Recommended Standard EIA-548, Electronics Industries Association, Washington, D.C., 1989.
- (3) Vantage Analysis systems Inc., VantageSpreadSheet.

Generation of Schematics and VHDL Descriptions of VLSI Layouts

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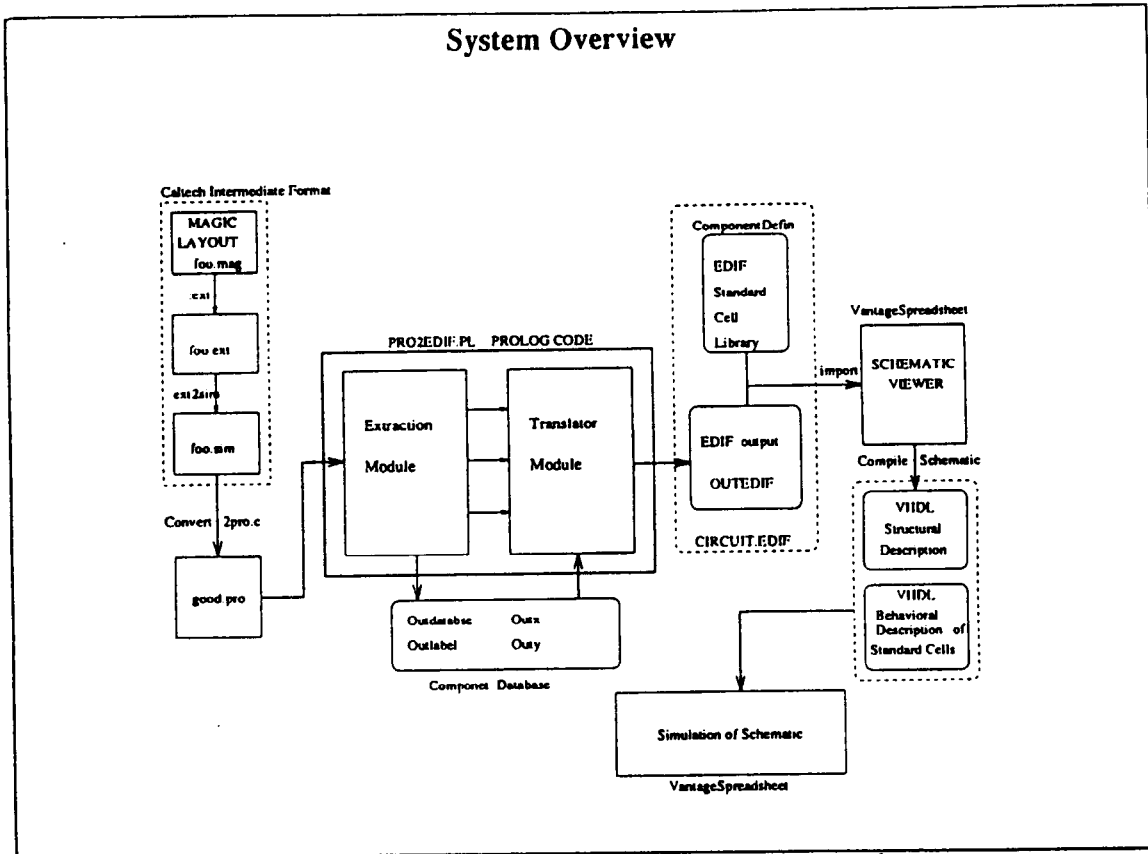
Overview

- System Overview
- Extraction Module: Logic Extraction of layout
- Preparing interim database
- Electronic Design Interchange Format (EDIF)
- Translator module
- Sample Circu associated and VHDL structural code
- Conclusions and future work.

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System Overview



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Extraction of Components

Transistor Netlist in Prolog Fact Form

p(nbin,nb,nvdd,3,3,-9,77,1).

n(nbin,ngnd,nb,3,3,-9,50,1).

p(nain,na,nvdd,3,3,-10,22,1).

n(nain,ngnd,na,3,3,-10,-5,1).

Extraction Rule For an Inverter:

inv :-

ptrans(G,D,nvdd,X1,Y1,Dr1),

ntrans(G,D,ngnd,X2,Y2,Dr2), Dr1 == Dr2,

remove_p(G,D,nvdd),

remove_n(G,D,ngnd), X is (X1 + X2)/2, Y is (Y1 + Y2)/2,

asserta(inv(X,Y,[G,D],[],Dr1)), fail.

inv.

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Sample 'outdatabase' File

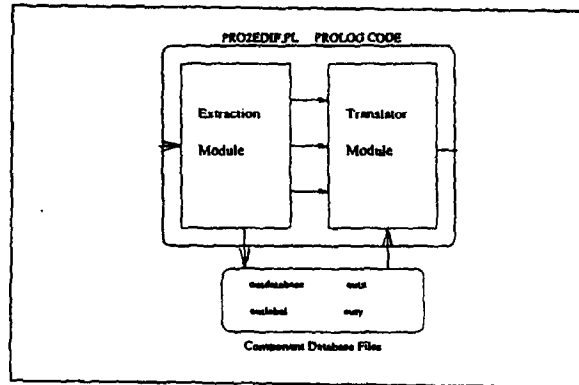
The 'outdatabase' File :

inv(0,-9,64,[nbin,nb],1).

inv(0,-10,8,[nin,nout],1).

tgate(1,79,78,[nout1,nclk, nclkbar,ngateout]).

nand2(3,16,50,[na,nb,nout1]).



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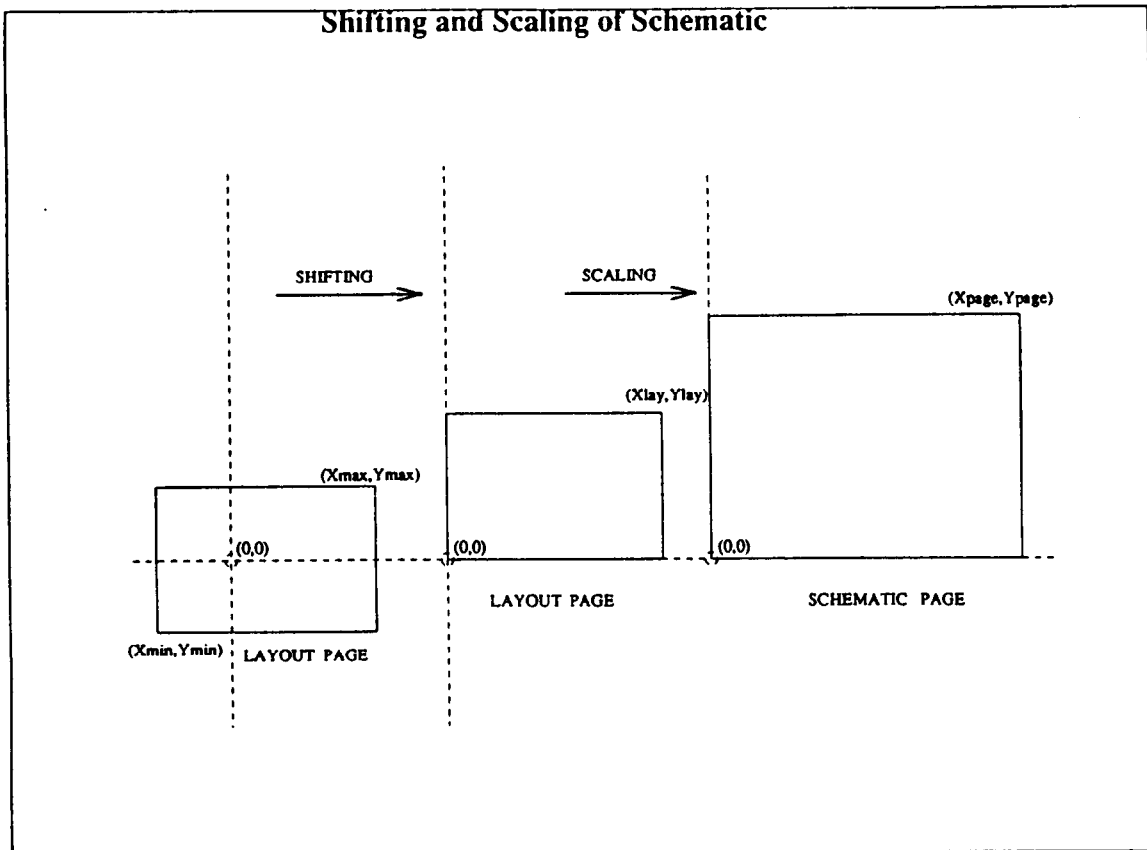
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Finding Primary Inputs/Outputs of The Circuit

- Automatic identification of primary input, primary output, and internal signals
- Prolog rules prepare and compare various label lists
- *InList*: A list of all unique input labels of the circuit
- *OutList* : A list of all unique output labels of the circuit
- *LabelList*: A list of all unique input and output labels of the circuit
- Primary input: associated label is present only in *InList*
- Primary output: associated label is present only in *OutList*
- Internal signal: associated label is present in both *InList* and *OutList*

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Shifting and Scaling of Schematic



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Electronic Design Interchange Format (EDIF)

- A textual format representing design
- Design description in a structured, hierarchical manner
- Define-before-use: local and external libraries
- One or many designs/libraries in one file
- EDIF file read/written by a database translator
- Cells , viewtype : Schematic,Netlist,Masklayout, PCBlayout
- Set of EDIF constructs depending upon the nature of information that is to be conveyed in the design
- Library ComponentDefin for cell definitions

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Format Of A Cell Instance

```

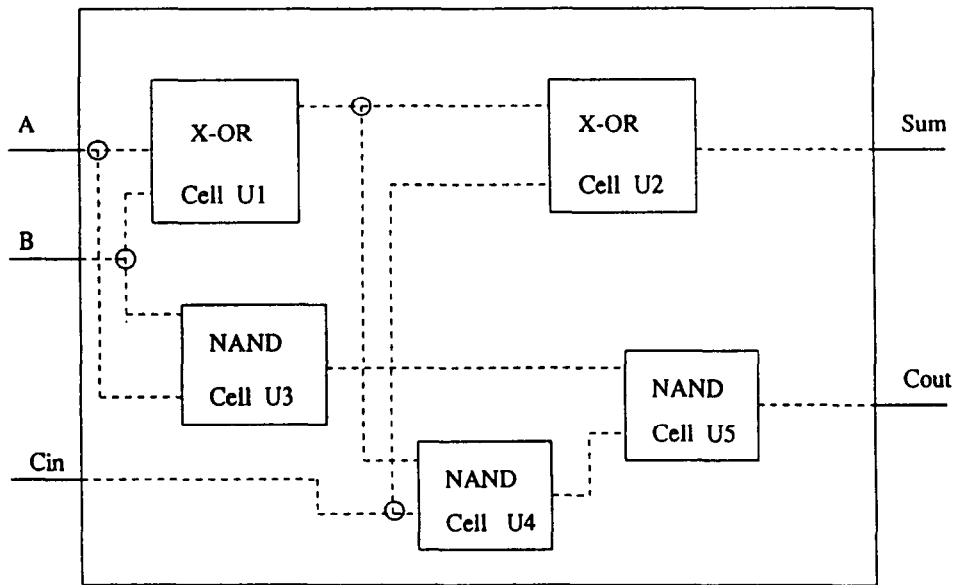
(cell circuit
  (view
    (viewType schematic)
    (interface
      (port ....)
      (port ....))
    (contents
      (instance ..... (cellRef .....))
      (instance ..... (cellRef .....))
      (net SignalName
        (joined
          (portRef ...(instanceRef .....))
          (portRef ...(instanceRef .....)))
        (figure SIGNALS
          (path .....))
        )/* end of net */
      )/* end of contents */
    )/* end of view */

```

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Top Most Cell - Circuit (Full Adder)



Top most cell - Circuit (Full Adder)

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VHDL Attributes For Each Cell

- VHDL attributes needed for circuit simulation
- Each port in a cell definition is assigned several attributes
- EDIF construct *property* associates attributes to ports
- Attribute VHDL_TYPE :
bit, byte
- Attribute VHDL_PORT_MODE :
in, out, inout, buffer

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Prolog Rule To Create Cell Instances

```
create_instance(inv(_,X,Y,[P1,P2],Dr),No, [Xs,Ys,Xf,Yf]) :-  
    get_name_points(inv,X1,Y1,X2,Y2,X3,Y3),  
    Xco is ( X + Xs ) * Xf ,  
    Yco is ( Y + Ys ) * Yf ,  
    round2five(Xco,Xcomp),  
    round2five(Yco,Ycomp),  
    BoxX is Xcomp + 70 , BoxY is Ycomp + 40 ,  
    assertz(box(Xcomp,Ycomp,BoxX,BoxY,inv)),  
    write_instance(No,inv,Xcomp,Ycomp,X1,Y1),  
    write_transform(Xcomp,Ycomp),  
    write_port_instance(ip,Xcomp,Ycomp,X2,Y2),  
    write_port_instance(op,Xcomp,Ycomp,X3,Y3).
```

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Describing Nets Of The Circuit

Writing Net For Signals Of The Circuit:

- net shows signal connectivity among components
- EDIF construct *joined*: for all signals; shows logical connectivity among ports
- EDIF construct *figure*: only for internal signals; signal connectivity is shown graphically
- i/o port symbols for primary inputs and outputs

Prolog Structures To Store Net-Database:

- `label_node_comp(control1,[ip,5]).`
- `label_node_comp(control1,[ip,13]).`
- `netlistof(control1,[[[470,130],i],[[620,25],i]]).`
- `netlistof(np,[[[110,540],x],[[380,135],i],[[435,550],i]]).`

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Sample EDIF Connectivity

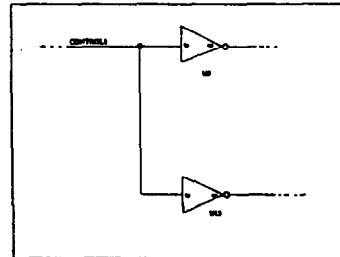
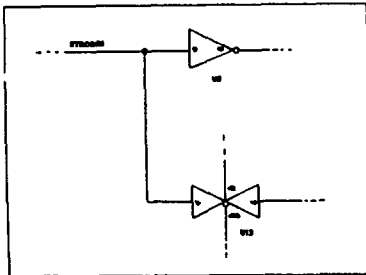
(joined

(portRef ip

(instanceRef U5))

(portRef ip

(instanceRef U13)))



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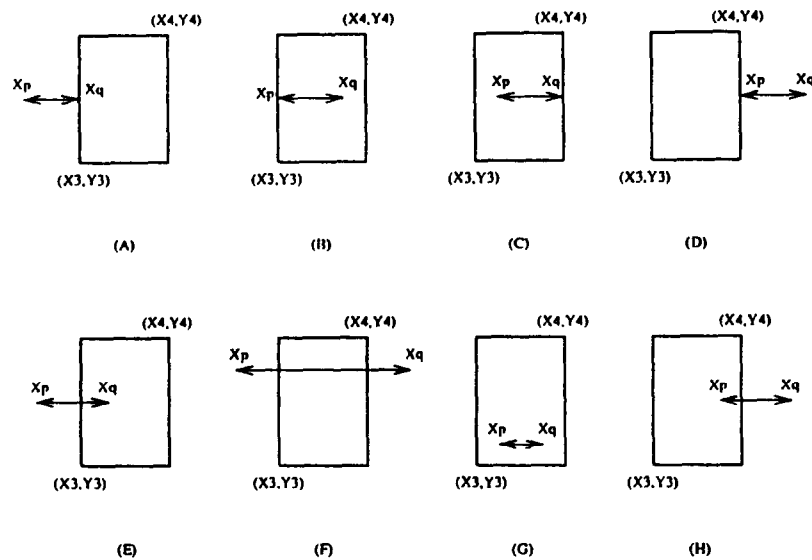
Routing Algorithm

- The schematic page is seen as a grid with horizontal and vertical spacing of 5 pixels
- Takes pointlist for one internal signal and draws graphical path connecting them
- A path between two points: Algorithm recursively and alternately draws horizontal and vertical lines along the grid (grid routing)
- Checking for line overlap
- Checking for box overlap
- Vertical and horizontal deadlock are avoided

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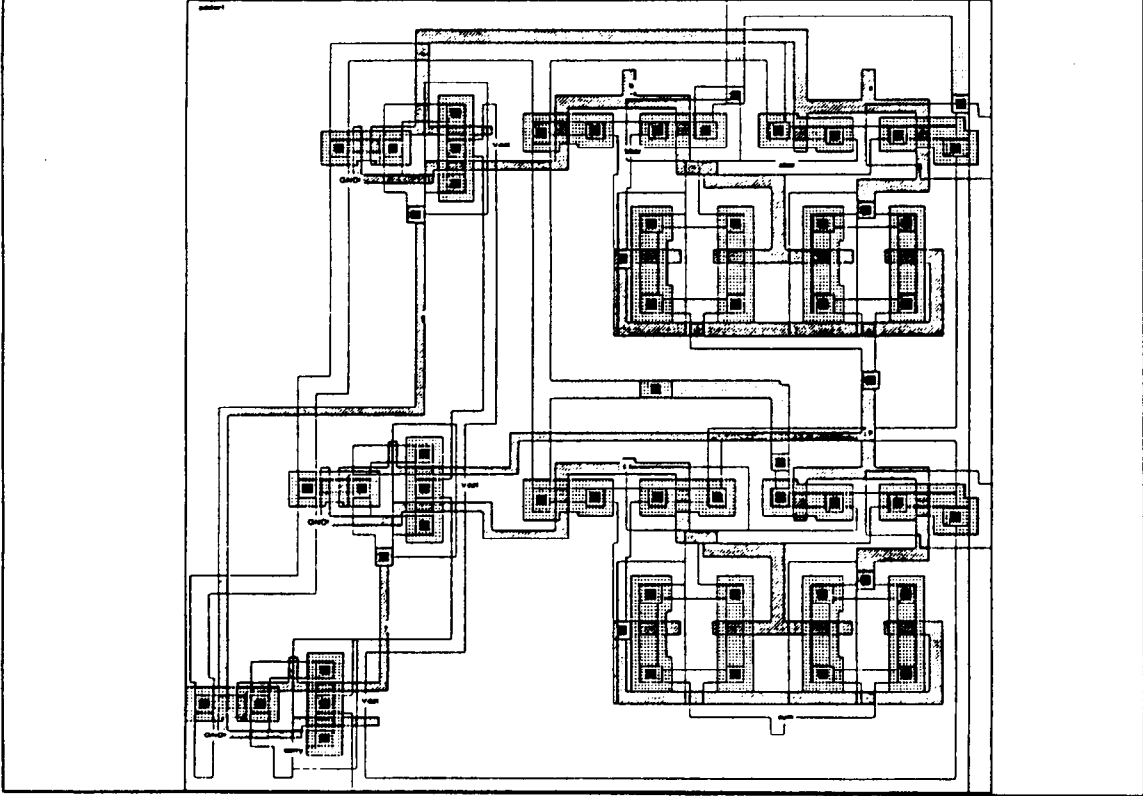
Possible Cases of a Box Overlap



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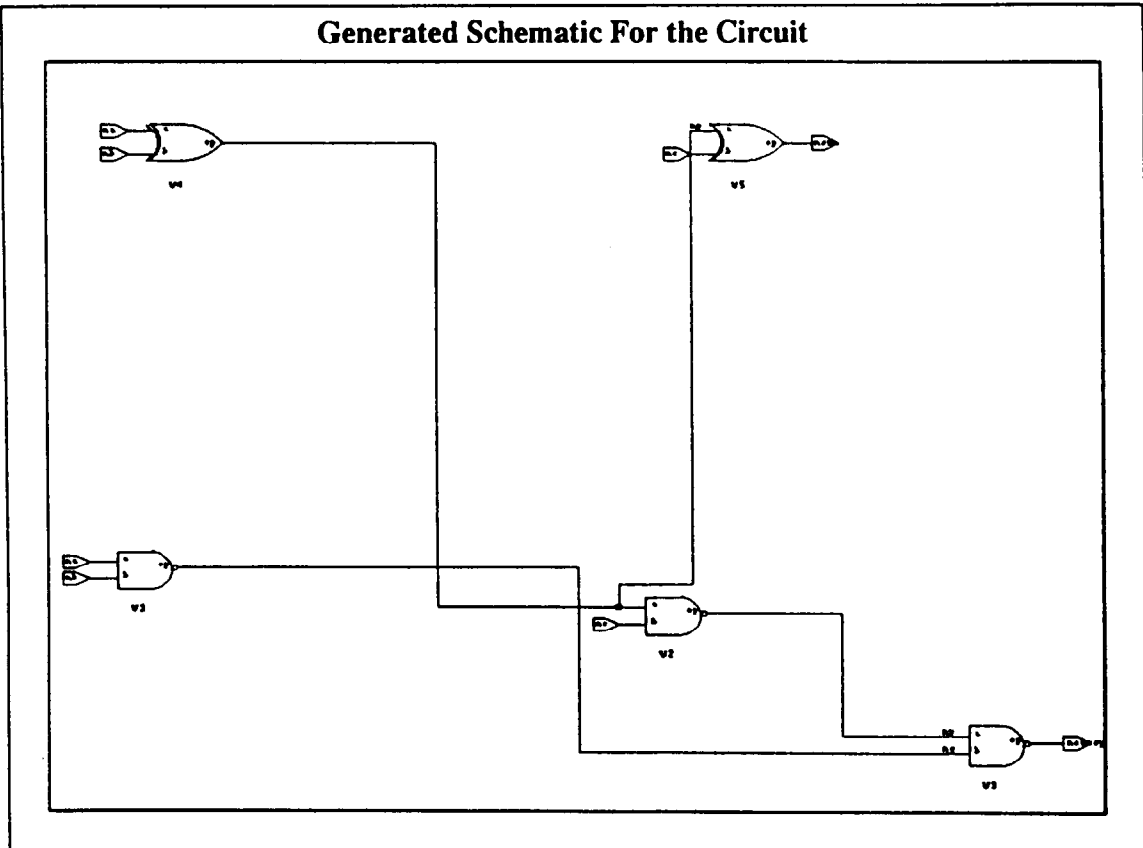
Layout of A Full Adder Circuit



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Generated Schematic For the Circuit



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VHDL Code For a Full Adder

```
USE std.std_logic.ALL;
ENTITY circuit IS
--$ !VANTAGE_METACOMMENTS_ON
PORT
(
ncarry: OUT bit;
nsum: OUT bit;
na: IN bit;
nb: IN bit;
nc: IN bit
);

END circuit;

LIBRARY TEMP;

USE std.std_logic.ALL;
ARCHITECTURE circuit OF circuit IS
--$ !VANTAGE_METACOMMENTS_ON
COMPONENT xor_gate
PORT
(
b: IN bit;
a: IN bit;
op: OUT bit
);

END COMPONENT;
COMPONENT nand2
PORT
(
op: OUT bit;
a: IN bit;
b: IN bit
);

END COMPONENT;

FOR U5:xor_gate
USE OPEN;

FOR U4:xor_gate
USE OPEN;

FOR U3:nand2
USE OPEN;

FOR U2:nand2
USE OPEN;

FOR U1:nand2
USE OPEN;
SIGNAL ng: bit;
SIGNAL np: bit;
SIGNAL ny: bit;

BEGIN

U5: xor_gate
PORT MAP (
op => nsum,
a => np,
b => nc );

U4: xor_gate
PORT MAP (
op => np,
a => na,
b => nb );

U3: nand2
PORT MAP (
b => ng,
a => ny,
op => ncarry );

U2: nand2
PORT MAP (
b => nc,
a => np,
op => ny );

U1: nand2
PORT MAP (
b => nb,
a => na,
op => ng );

END circuit;
```

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Conclusions

- Extraction of standard layout.
- More components can be extracted, multi-sheet schematic.
- Circuit documentation in form of EDIF schematic
- EDIF - an industry wide standard for documentation
- Portability to various VHDL based Design Environments such as VantageSpreadsheet
- Generation of VHDL structural architecture
- Simulation of schematic at gate level

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