

A VHDL ASIC Library for MOSIS Fabrication with Back Annotated Delays

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ABSTRACT:

There exists a prevalent need of VHDL models for the MOSIS community involved in ASIC design. The accuracy of today's simulations using data book values is not sufficient to provide results comparable to actual chip testing. The technique discussed here describes a method using back annotated data to calculate proper delays based on the input rise and fall times along with the output capacitive loading for each cell. This data, when combined with the generics Tech, Model, Temp, and Vdd, provide the timing formula with the necessary parameters to calculate the delay for each input to each output. This calculation is performed at elaboration time for the models based on those generics. Currently, there are four supported conditions based on Technology, Temperature, Voltage, and Process: Nominal (1.2u, 25 Celsius, 5.0 volts, TNTP), Best (1.2u, -55 Celsius, 5.5 volts, FNFP), Worst (1.2u, 140 Celsius, 4.0 volts, SNSP), and Low Voltage (1.2u, 80 Celsius, 2.0 volts, SNSP). The ability to support other conditions is available with future characterization. Proposed plans include support for 0.8 micron technology.

Characterization Data Extraction: SPICE simulations are performed on the models for each set of environmental conditions under a variety of loads. Data for the different load conditions is then extracted from the SPICE results and ported to Mathematica. The data is then curved fit to a timing formula and the coefficients for the formula are extracted. The VHDL Data files containing the coefficients for each environmental condition are then automatically generated for the cell.

Back Annotation: Capacitive loading is extracted from the netlist for each cell and the input transition times associated with the cell are calculated. This information is then inserted as generics in the structural models. The structural models can then be compiled with the overloaded generics providing accurate back annotated timing models.

Behavior: The models are written to comply with VHDL 1076-1987 and use the IEEE 1164 logic system. The behavior of each cell is independent of the environmental conditions imposed on it. The timing for the cell, however, varies with these conditions. The user has the ability to set generics for different conditions of technology, temperature, voltage and process. The user also can select whether to display assertions and/or propagate unknowns for timing violations.



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Introduction

Program:

DARPA Embedded Systems: Contract # 110-1-1002-4

Project:

VHDL Modeling Specification for a Scalable CMOS MOSIS Standard Cell Library

Problem:

Lack of VHDL models for the MOSIS community involved in high-performance digital ASIC design.

Traditional logic simulation of semi-custom ASICs involves worst case data book timing.

Objective:

Create VHDL models for the CMOS Library that will exhibit accurate Model vs Device Behavior



Library Overview:

- Library modeled is dlmV3.0 SCMOS Library.
 - Contains 68 cells composed of combinational, sequential, tri-state, and other cells
 - Lager IV toolset plans to support this library

Project Approach:

- Models must be VHDL-1076 compliant and use IEEE-1164 multi-value logic system
- Models must be able to share a common timing formula that is customized by a cells data structure and generics
- Delays must be calculated at elaboration to speed up simulations
- Ability to add support for other environmental conditions as data becomes available
- Ability to upgrade the data structures with more accurate data

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Project Tasks

1. Characterization Data Extraction
2. VHDL Behavioral Models
3. Back Annotation Software
4. Verification of Library
5. Model vs Device Testing



Characterization Data Extraction

- **SPICE simulations are performed on a cell for each set of environmental conditions under a variety of loads**
- **Data is extracted from the SPICE simulations**
- **The SPICE data is ported to Mathematica where it is curve fit to a timing formula and the coefficients extracted**
- **VHDL Data files containing the coefficients for each environmental condition are then automatically generated for the cell**
- **The back annotated generics (environmental conditions, input transition times, and output capacitive loading) and characterization data structures are used to calculate the delays at elaboration time**

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VHDL Behavioral Models

- **VHDL-1076 compliant models using the IEEE-1164 multi-value logic system**
- **Generics are used to**
 - **back annotate input transition times**
 - **back annotate output capacitive loading**
 - **select environmental conditions to simulate under**
 - **display assertions and/or propagate unknowns for timing violations**
- **Delay calculations are performed at elaboration time**
- **General Modeling Scheme: Calculate delays at elaboration, determine function, determine delay to use**



Back Annotation Software

- Calculate for Each Cell
 - input transition times
 - output capacitive loading
- Data Annotated into VHDL Structural Model
- User Run-Time Selection
 - environmental conditions
 - simulation options
- CAD Tool Interface
 - Phase I: Mentor Graphics Design Architect Software
 - Phase II: Generic EDIF Interface

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Verification of Library

- Developed Verification Procedure and Checklist
- Key features of MPL's Model Verification Procedures and Checklist
 - Customized checklist for each model
 - All VHDL code, test vectors, and simulation results are embedded within the Verification Document
 - Check boxes for completed tasks



Model vs Device Testing

- Design a test chip
- Fabricate the test chip through MOSIS
- Test the returned chip
- Examine Model vs Device data for accuracy of the models

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Summary

- Supported Conditions at this time include the following:
 - Best (1.2u, -55C, 5.5v, FNFP)
 - Nominal (1.2u, 25C, 5.0v, TNTP)
 - Worst (1.2u, 140C, 4.0v, SNSP)
 - Low Voltage .. (1.2u, 80C, 2.0v, SNSP)
- Proposed plans include support for 0.8 micron technology
- Results comparable with SPICE simulations