

## **Project Update: Design of an Airborne Graphics Generator**

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### **ABSTRACT**

"Situational awareness" has been identified as the single most critical factor in improving mission effectiveness in fighter aircraft. Situational awareness can be described as having knowledge of the current and near-term disposition of both friendly and enemy forces within a volume of space. This knowledge or information in future military aircraft will be presented in the cockpit using computer or electro-optically generated displays. Thus, display technologies are critical for providing a pilot the situational awareness necessary to fly, fight, and survive in the future combat environment.

This paper will present a status update on the Airborne Graphics Generator project for future cockpit display technology. Discussion will include an overview of plans of the Cockpit Avionics Office to generate through current and future air force contracts, in co-operation with in-house research at the Cockpit Avionics Office, a system level VHDL simulation of the Airborne Graphics Generator. VHDL design practices and model availability with proprietary information protection are major points of this paper.

This paper will provide an excellent opportunity to inform government agencies, DOD contractors and the VHDL design community of a design example (the Airborne Graphics Generator) of top down design methodology for VHDL design that is working. As the Department of Defense (DOD) budgets shrink, less flight testing will be possible, forcing the DOD to do more simulation to verify accuracy. VHDL provides an excellent platform for these system simulations.

Fall VUG Conference 90 (Oakland, CA):

1. - A VHDL Simulation of an Airborne Graphics Generator (Myers:WL/AAA-2)

Fall VIUF 91 (Newport Beach, CA):

2. - VHDL Architectural Assessment (Rose, Carpenter, Steeves: Honeywell SRC)

Fall VIUF 92 (Washington, D.C.):

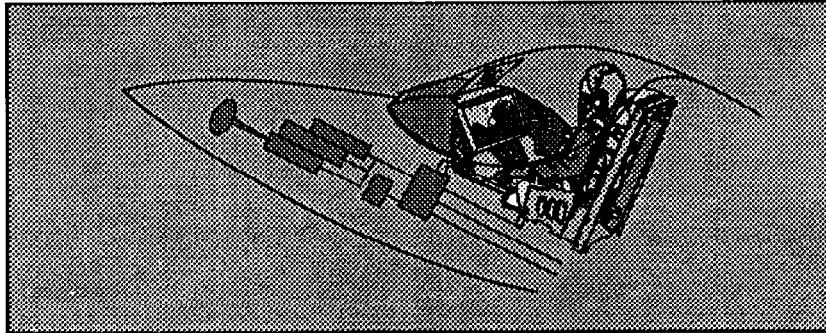
3. - Using VHDL as a System Specification (Honeywell SRC)
4. - Performance Modeling with VHDL (Tutorial, Honeywell SRC)
5. - Development of i960 Processor Models to Support Hardware/Software ... (OSU)
6. - High Speed Communication for Simulation of Large VHDL Models (UC)
7. - A Parallel, Optimistically Synchronized VHDL Simulator Executing on a ... (UC)

\*\* See Also Documentation Charts at end of this paper.



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Oct 92 : Fall VIUF Meeting



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WL/AAA-2

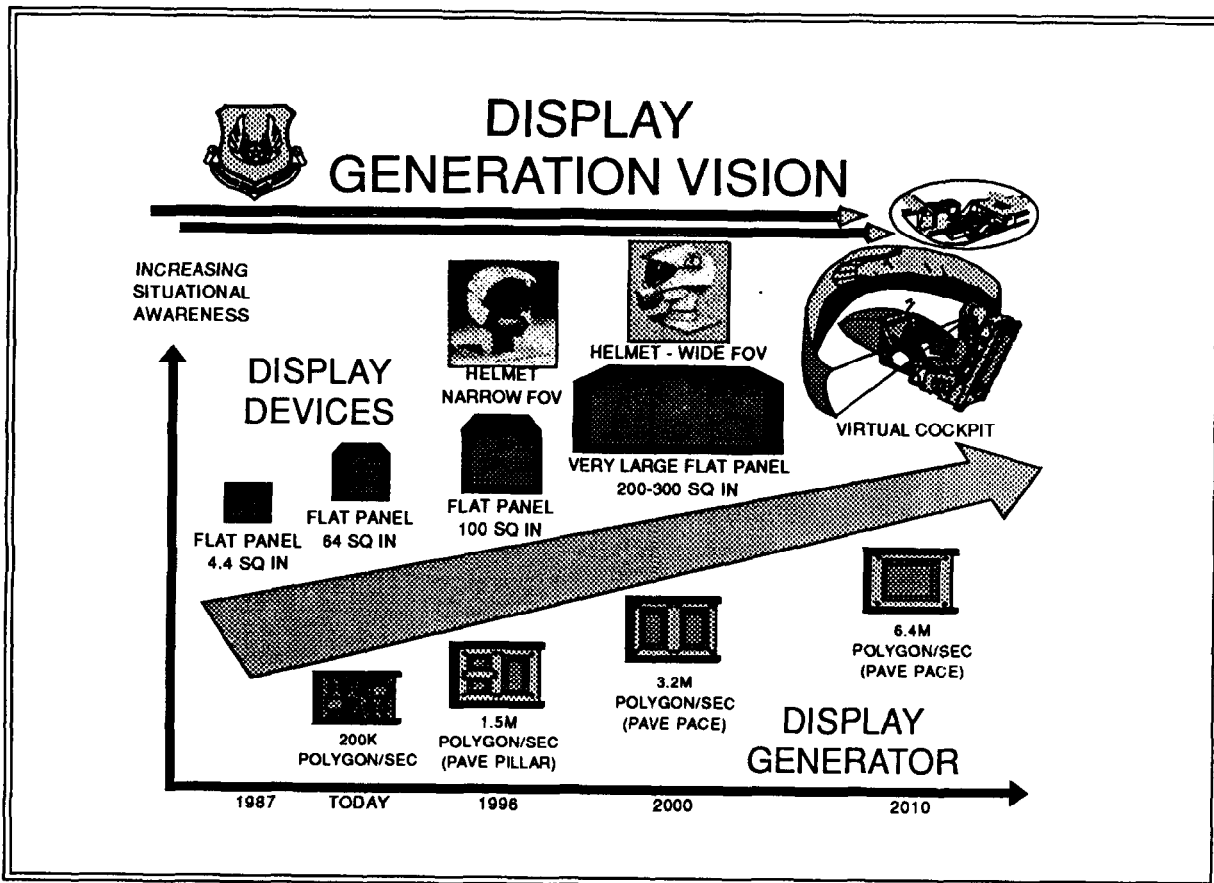


## Presentation Outline

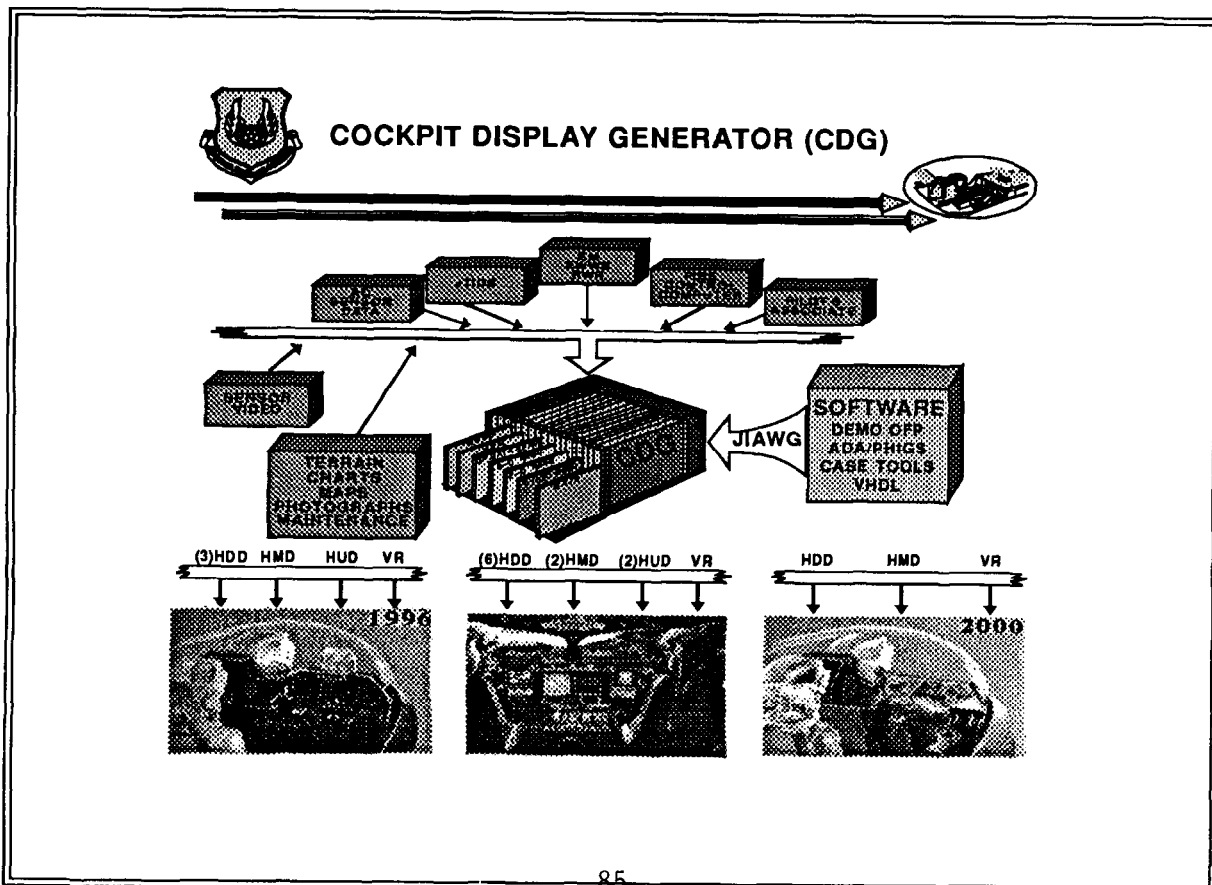
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- **Display & Graphics Technology Vision**
- **Cockpit Display Generator (CDG) Program**
- **VHDL Research**
  - **Intel CAP32 processor Model (OSU)**
  - **Distributed VHDL Simulation (UCVHDL)**
  - **JIAWG Bus Models (HSDB) (NOT Presented)**
- **Research Goals FY93 - FY95 (NOT Presented)**
- **Documentation (NOT Presented)**

WL/AAA-2



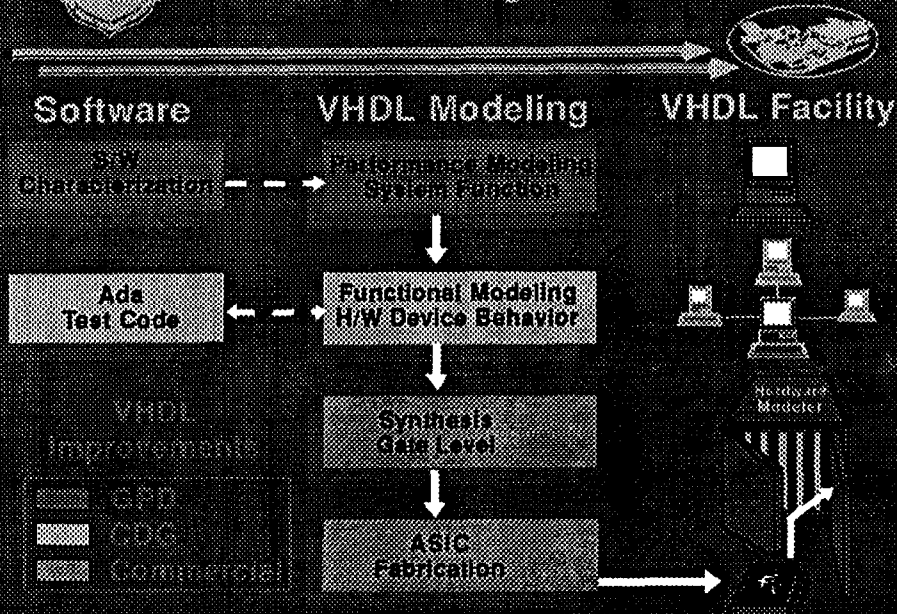
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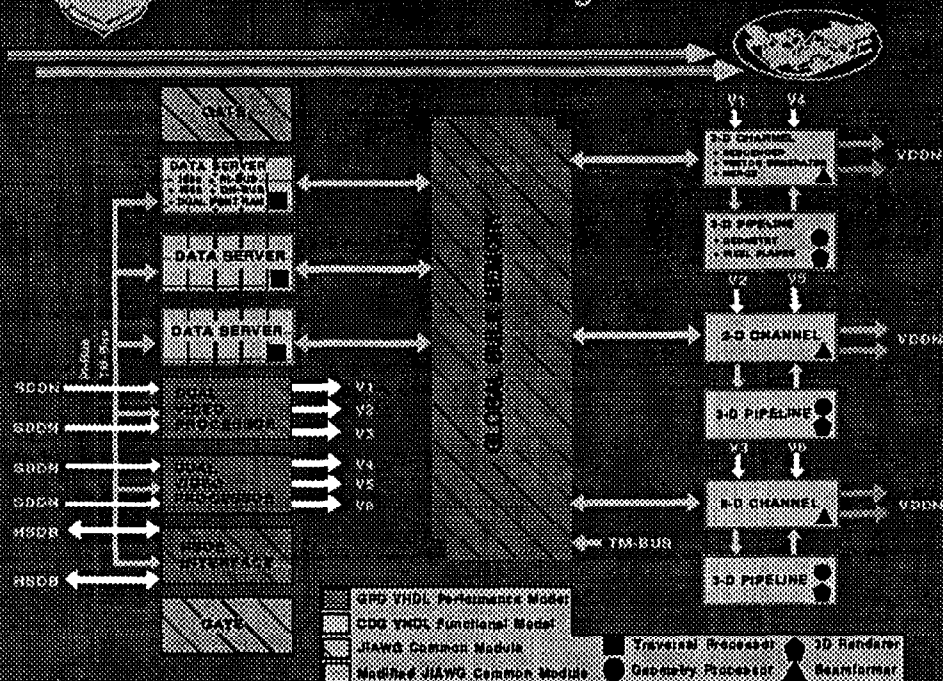
WL/AAA-2



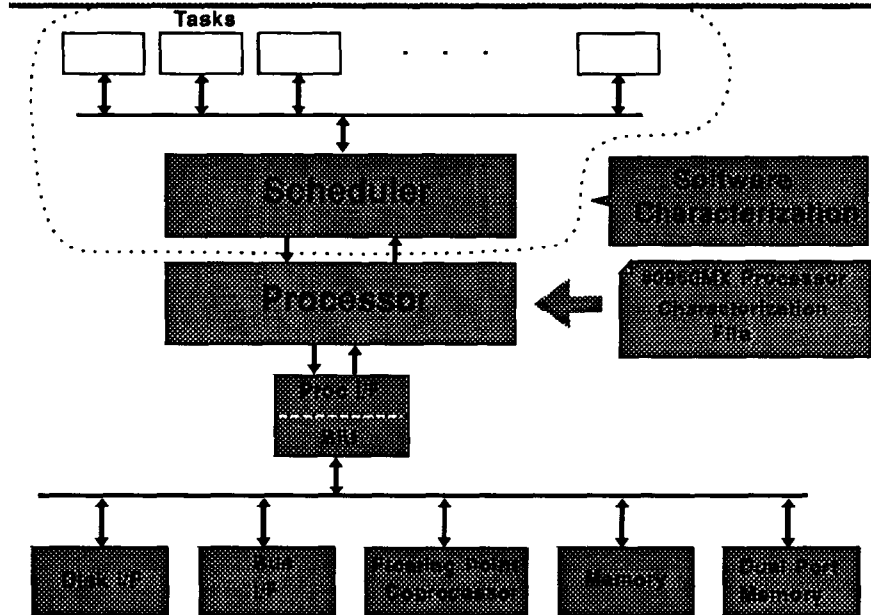
# COCKPIT DISPLAY GENERATOR (CDG) VHDL Design Process



# COCKPIT DISPLAY GENERATOR (CDG) Architecture/VHDL Design/Common Module



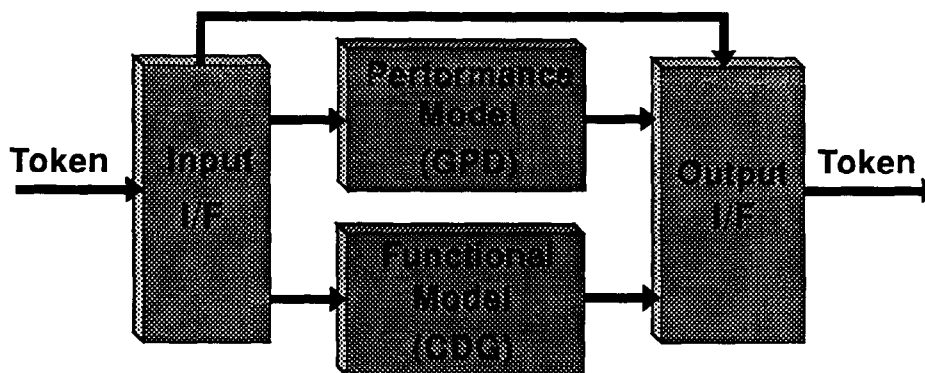
# GPD Processor Model



WL/AAA-2



# Hybrid Modeling



- Input I/F – breaks down token and sends to model
- Output I/F – Converts outputs back to a token  
- Compares Latency results of two models

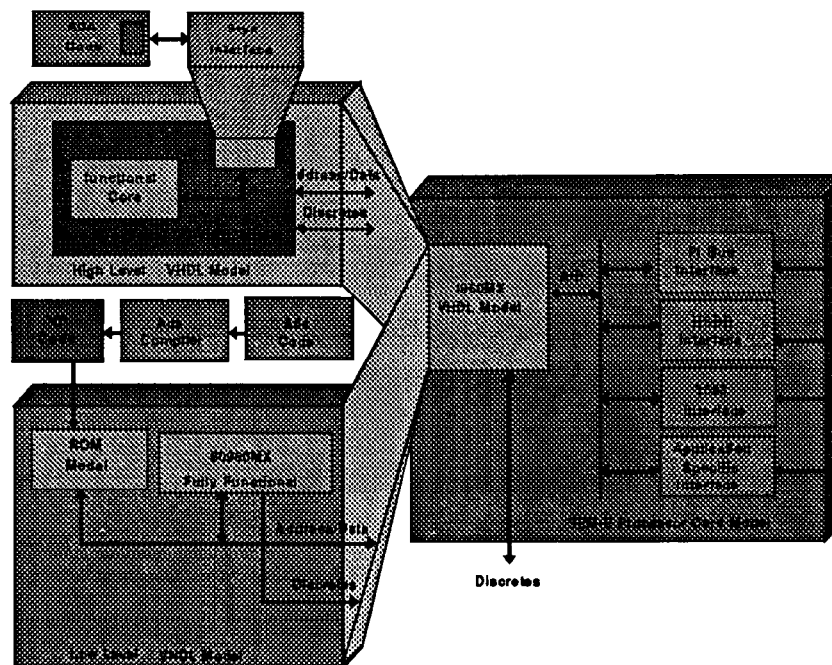


## Cap32 Processor Research

- Contractor: Ohio State University (OSU)  
Principal Investigator: Dr Joann DeGroat  
Staff: (2) M.S. Engineering Students at OSU
- Contract delivers two Cap32 models:
  - 1) a "Bus Functional" model with Ada interface using Vantage "Styx" C code Interface
  - 2) a "Fully Functional" model (opcode executable) through use of Meridian Ada Compiler
- Implementation of "*Software Intensive Hardware*" memo
- The Cap32 processor model will provide for Executable Ada Code *INSIDE* a VHDL Simulation
- Investigation of Vendor "*Proprietary Data*" Protection in a Public Domain VHDL Model

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## Intel i960MX VHDL Model Breakdown





## Distributed VHDL Simulation

- **Contractor: University of Cincinnati (UC)**  
**Investigators: Dr Hengen & Wilsey**  
**Staff: (2) Ph.D. Engineering Students at WPAFB**  
**AFOSR Support: (1) M.S. Engineering Student at WPAFB**
- **Contract Delivers DARPA funded QUEST Software from UC to WPAFB with enhanced performance upgrades**
- **Needed for Execution of Large VHDL models delivered by CDG program**
- **Up to 60X improvement in execution speed of VHDL simulation over single HP or Sun workstation**
- **Simulation Speed equivalent to or exceeds current "Behavioral Accelerators" on the Market.**

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## Distributed VHDL Simulation

- **Enhancements to be Added to QUEST Software:**
  - **Automated Partitioning of VHDL Simulation**
  - **Use of Fiber-Optic Bus (SCRAMNET)**
  - **Process Migration: Reconfigure as Workstations needed**
- **Extracts VHDL Designs from the "Vantage Spreadsheet"**
- **Algorithms applied are:**
  - **Non-Deterministic Simulation**
  - **Time Warp**
  - **Shared Memory Data Structures**

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## JIAWG Bus Models

- **High Speed Data Bus (HSDB)**  
MS Thesis Project (Jun 92 – Jun 93)
- **Functional Modeling in support of CDG**
- **Benchmark for implementation of JIAWG Bus Specs**
- **Working with ASC and SAE Standards working Groups for Definition of JIAWG and commercial standard.**
- **Allows functional level testing of graphics architecture**

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## CDG VHDL Simulation Research

### Goals (Future Research)

- **VHDL**
  - **Distributed VHDL Simulation (Continued)**
    - **Process Migration**
    - **Graphical Interface w/Vantage Spreadsheet**
  - **JIAWG**
    - **High Speed Data Bus (Continued)**
    - **Pi Bus**
    - **Transition TM Bus from ARMY**
  - **i960MX**
    - **Testing of Model .vs. fabricated ASIC**
  - **Synthesis of CDG ASICs**
- **PCCADS+**
  - **Air-to-Ground Mode**
  - **update to CDG formats**
  - **VHDL Interface**
- **Video Compression/Decompression**

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## **CDG VHDL Simulation Research Documentation**

- **GPD Final Report (McAir)**
- **GPD Final Report (Honeywell SRC)**
- **PCCADS+ Final Report (Vol III) (McAir)**
- **A VHDL Simulation of an Airborne Graphics Generator (Myers-90)**
- **VHDL Design and Simulation for Airborne Graphics Generation Requirements (Myers-91)**
- **A VHDL Performance Modeling Environment (Honeywell-91)**
- **Architectural Assessment with VHDL (Honeywell-91)**

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## **CDG VHDL Simulation Research Documentation FY 92**

- **VHDL as a Specification Language (Myers-92)**
- **Using VHDL as a System Specification (Honeywell-92)**
- **Performance Modeling with VHDL (tutorial) (Honeywell-92)**
- **Issues with Hardware/Software Co-Design (Honeywell-92)**
- **Development of I960 Processor Models to support Hardware/Software Co-Design (OSU-92)**
- **High Speed Communication for Simulation of Large VHDL Models - (UC-92)**
- **A Parallel Optimistically Synchronized VHDL Simulator Executing on a Network of Workstations (UC-92)**
- **Distributed Simulation on a Reconfigurable Network using Non-Uniform Message Passing (UC-92)**

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