Mapping Conceptual Graphs to VHDL Descriptions

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Abstract

A conceptual graph is a method of storing knowledge. Using this data structure it is possible to store block diagrams, timing specifications, behavioral descriptions, and more. Using conceptual graphs to store the behavioral description of a device it is possible to create a VHDL description of the device in the form of a process model graph. Sentences describing the behavior of a device can be analyzed and put into the form of conceptual graphs. These would then be joined into one graph which would describe the device's overall behavior. This graph would be, in effect, a list of all the actions which the device performs and the conditions under which they operate. It is now possible to use this to create a VHDL behavioral model of the device. Each action performed by the device could be mapped into one or more processes acting upon signals running between those processes. This Process Model Graph (PMG) could then be edited in order to fill in any holes that might be left by the interpreter, and then combined into a VHDL Entity ready for simulation.
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to VHDL Descriptions

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OUTLINE

ASPIN - Automated Specification Interpreter

Conceptual Graphs

CGVHDL - The Prototype Linker

Limitations and Suggested Improvements

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ASPIN
Automated SSpecification INterpreter

Ultimate goal - Reduce the design cycle time and cost
Method - Create a behavioral system model from informal specifications

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The ASPIN System

PARSER

SEMANTIC ANALYZER

MODEL GENERATOR

C.G. PROCESSOR

VHDI LINKER

MODELER'S ASSISTANT

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English to Conceptual Graph Example

'The 8-bit data is loaded into the ACC register when STRB rises.'

CGVHDL
The Prototype Linker
CGVHDL Interpretation Strategy

1. Separate action concepts from object concepts
2. Distinguish actions from conditions
3. Determine behavior from the graph
4. Interpret an object's graph as a VHDL signal or value
5. Retrieve the VHDL from the databases

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Interpreting a Graph
LIMITATIONS

Only interprets behavior - not structure
Only one condition per action
Port modes remain unidentified
IMPROVEMENTS

Allow devices to generate processes
Allow multiple conditions
Identify port modes
Allow editing and merging of processes before writing a PMG

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