

**Using VHDL Design Synthesis to
Create Producing LSI for DoD**

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ABSTRACT

VHDL can help contractors meet two objectives: reduction of LSI design cycle time and generation of technology independent models to satisfy DoD requirements. If synthesizable RTL VHDL is written following certain design rules, logic-optimized producible LSI can be efficiently designed. VHDL provides the advantages of reusability and documentation. RTL simulations should match LSI tool generated simulations.

RTL VHDL was written to model JTAG control logic and some cryptographic algorithms which already existed as LSI hardware. Inputs for the JTAG VHDL test bench were created with JTAG design tools. The RTL logic simulations matched those obtained with typical LSI design tools. A gate level VHDL library of the LSI cell family was constructed so that synthesized code could be compiled, simulated, and checked for consistency to RTL simulation. Potential hazards in the process were identified, design rules for writing synthesizable and simulation-compatible RTL code were formed, and an RTL to gate level conversion methodology was created.

ACKNOWLEDGEMENTS

Bill Oh of MOTOROLA GEG for valuable knowledge about designing producible LSI.

REFERENCES

1. Synopsys, Inc., "VHDL Compiler™ Reference," 1098 Alta Ave., Mountain View, CA, 94043. (415) 962-5000.

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VHDL Simulation Levels

Behavioral – System and/or software simulation
Register Transfer Level – Clocked elements and logic
Structural – Netlist

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Structural vs RTL

Structural

- Real gates (Timing)
- Fault grade
- Portable to other netlist formats

RTL

- Readable
- Portable to various technologies
- Compatible with LSI tools

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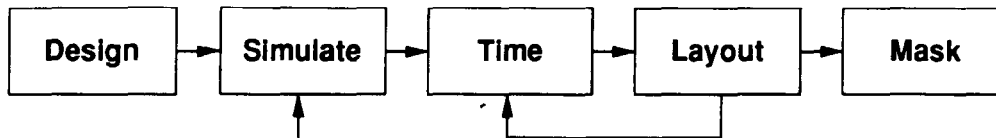
Advantages of RTL Synthesis

- Speed-up over traditional design method
- Early validation
- Documentation requirements
- Portability to various technologies
- Optimize for speed, area...

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DoD Quest for Ownership

Old LSI Design Cycle



New cycle can end here initially or in future production

- Solves second source problem
- Lower cost due to competition

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Disadvantages of Synthesis

- Complicated schematics
- Fan-out problems, clock trees
- Lose "human touch"

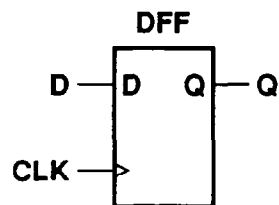
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Hazards of Poor RTL Code

- Extra latches
- Gated clocks
- Reverse modularity
- Won't match LSI tool simulations

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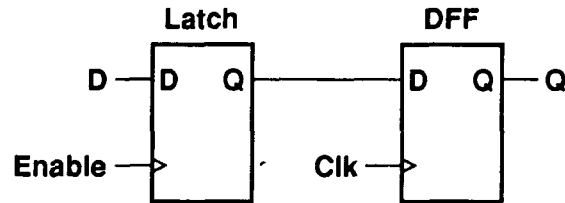
Inferring Edge Triggered Elements



```
if (clk' event and clk = '1') then
  Q <= D;
end if;
```

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D-Flop Preceded by a Latch



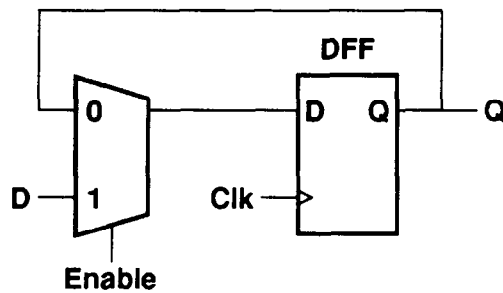
```

If (clk' event and clk = '1') then
  If (enable = '1') then
    Q <= D;
  end If;
end If;

```

11168-41

Scan-Flop



```

If (clk' event and clk = '1') then
  D <= D;
  If (enable = '1') then
    D <= Q;
  end If;
end If;

```

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Unknown vs "Don't Care"

- LSI simulators assign 'X' to unknown signals
- Hardware shouldn't be designed to assign 'X' conditions

Solution

1. Assign X in simulation
2. Comment out for synthesis

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Propagating 'X' Conditions

```
if (sel = '0') then
    out <= in1;
elsif (sel = '1') then
    out <= in2;
else
    out <= 'X';
```

```
if (sel = '0') then
    out <= in1;
elsif (sel = '1') then
    out <= in2;
elsif (in1 = in2) then
    out <= in1;
else
    out <= 'X';
```

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Using Synthesizer Constraints

$$\text{Cost} = \sum_{i=0}^n L_i D_i$$

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Results of Good Methodology

First Run

1752 cells

Second Run

1100 cells

**Good compare on structural
VHDL simulation**

11168-06

Porting the Design RTL

JTAG Model

- Two cell family targets
- Seven different custom LSI

Pluses

- Compatibility
- Redundant effort eliminated

Minuses

- Clock constraint capability for mid-bit clocking

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Summary

VHDL provides:

- Documentation
- Portability
- DoD requirement satisfaction

Synthesis provides:

- Automation
- Optimization

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