Hazard Detection with VHDL in Combinational Logic Circuits with
Fixed Delays

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Abstract

Timing hazards are common problems found in logic circuits. A new integrated hazard detection system (HDS), which is implemented in VHDL, is proposed to detect the static, dynamic and function hazards in any logic circuit that is described structurally in VHDL. This system adopts the IEEE VHDL Model Standard Group 1076 - 1164 Nine-Valued Multiple-Valued Logic package. Without any designer-supplied arbitrary input test patterns, the system predicts which input combinations will cause hazards, reports what type of hazards, and provides detailed timing information on the hazards in the combinational logic circuit with fixed gate delays.
Hazard Detection With VHDL
In Combinational Logic Circuits
With Fixed Delays

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Agenda

1. Motivation

2. Overview of Hazards

3. The VHDL Hazard Detection System (VHDS)
   * Logic Package
   * Timing Package
   * VHDS Hazard Pattern Generator
   * Hazard Detection Package

4. Examples and Results Analysis

5. Conclusion
Motivation

Develop an integrated system that is capable of reporting common types of hazards and capable of predicting all input combinations that cause hazards for any test circuits that are described structurally in VHDL.

Introduction to Hazards

What is a hazard?

A hazard is a momentary output spike which differs from what is predicted by a normal stable state analysis.

-Cause
  * Unfavorable Input Combinations
  * Device Propagation Delays

- Effect
  * Circuit Malfunction (Can be Harmful)
Summary of Hazard

Definition of Hazards

Static 0 Hazard

Static 1 Hazard

Key:
* M-hazard: Multiple hazard, i.e., a hazard that is caused by more than one input change.
* Static hazard also called 1-variable logic hazard.

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Definition of Hazards

Dynamic 0 Hazard

Dynamic 1 Hazard

Definition of Hazards

Two Inputs Change Simultaneously
Function 0 Hazard

Two Inputs Change Simultaneously
Function 1 Hazard
K-Map Illustration of Hazards

Block Diagram of VHDS (VHDL Hazard Detection System)
Logic Value System for VHDS

Adopt IEEE VHDL Model Standard Group STD_LOGIC_1164
MVL9 nine-valued logic package

X: Unknown (Strong '0' or Strong '1')
0: Strong '0'
1: Strong '1'
Z: High Impedance
W: Weak Unknown
H: Weak '1'
L: Weak '0'
U: Uninitialized State
-: Don't Care State

Timing Design in VHDS

1. Delay Model:
   - Inertial Delay
   - Transport Delay
   - Delta Delay

2. Delay Parameters
   * Binary Delay
     - TP_01: Propagation delay from low to high
     - TP_10: Propagation delay from high to low
   * Tri-state Delay
     - TP_1Z: Propagation delay from high to high impedance state
     - TP_Z1: Propagation delay from high impedance state to high
     - TP_0Z: Propagation delay from low to high impedance state
     - TP_Z0: Propagation delay from high impedance state to low
   * Wire Delay
     - CONN_DELAY: Wire or metal delay between logic devices

Rise Delay
(Tri-state)

<table>
<thead>
<tr>
<th>I</th>
<th>H</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>L</td>
</tr>
</tbody>
</table>

Fall Delay
(Tri-state)

CONN_DELAY

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Type Conversion Functions

\[ \text{TIME} \leftrightarrow \text{NATURAL} \to \text{STRING (CHARACTER)} \]

assert condition
report IF & "Function 0 Hazard is detected on " & SIGNAL_NAME & " at " & NATURAL_TO_STRING(TIME_TO_NATURAL(HAZARD_TIME)) & "ns"
-- Assume the value of HAZARD_TIME = 1000 ns
severity WARNING;

Example: Function 0 Hazard is detected on OUTPUT at 1000 ns

Min and Max Propagation Delays Computation in VHDL Structural Model

The Longest and Shortest Delay Path Problem
Individual Component Self-Updating Technique

Key:
- Signal Unit
- Time Unit
- Time Bus Terminated Unit
- Timing Information
- Signal Connection

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Min and Max Propagation Delays Computation in VHDL Structural Model

The Longest and Shortest Delay Path Problem
Individual Component Self-Updating Technique

VHDL Component Description:
Example

```vhdl
component MODEL -- Component A
generic (TP_01, TP_10, DELAY_MODEL);
port (INPUT: in MVL9; OUTPUT: out MVL9; -- PROP_DELAY_SPEC: (min, max)
  TIME_IN: in PROP_DELAY_SPEC; TIME_OUT: out PROP_DELAY_SPEC);
```

VHDL Component Association

A: MODEL
generic map(5 ns, 5 ns, TRANSPORT_DELAY)
port map(INPUT => INPUT_1, OUTPUT => OUTPUT_1, TIME_IN => TIME_IN_1,
  TIME_OUT => TIME_OUT_1);

Overview of a Time Unit and a Time Bus Resolved Unit

(a) Internal Structure of a Time Unit

Time Set: = [(TP_01, TP_10, TP_02, TP_12, TP_01, TP_10, and CONN_DELAY]
Default: Time Set = [TP_01, TP_10]

MIN_TIME (Time Set) = MIN_TIME (TP_01, TP_10) and
MAX_TIME (Time Set) = MAX_TIME (TP_01, TP_10).

(b) Internal Structure of a Time Bus Resolved Unit
Flow Chart of Hazard Pattern Generator

Single-Input Change

Start

Input Specification
number of inputs

Generate a range of
naturals from:
{0, 1, 2, 3, ..., 2^N - 1}

natural to BIT_VECTOR

Each original bit pattern
is looking for all
possible neighbor bit
patterns that differ by
one bit.

Group the original bit
patterns and its neighbor
bit patterns
and re-organizes in the
form of two-tuples.

Inject the two-tuples
into the test circuit

End

Illustration of the Single-Input Change Two-Tuple Test Patterns

Single-Input Change
(a) 3-variable case:

<table>
<thead>
<tr>
<th>XY</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z</td>
<td>![2x2 Grid]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Each cell has three neighbor
cells which differs by one bit.
So, the total number of
test pattern = 8 x 3 = 24

(b) 4-variable case:

<table>
<thead>
<tr>
<th>AB</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD</td>
<td>![2x2 Grid]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Each cell has four neighbor
cells which differs by one bit.
So, the total number of
test pattern = 16 x 4 = 64

In general, the total number of patterns required for N inputs = 2^N * N
Flow Chart of Hazard Pattern Generator

Two-Input Change

Start

Input Specification
Number of Inputs

Generate a range of naturals from: [0, 1, 2, 3, ..., 2^n - 1]

Natural to BIT VECTOR

Each original bit pattern is looking for all possible first neighbor bit patterns that differ by one bit.

Each first neighbor bit pattern is looking for all possible second neighbor bit patterns that differ by one bit (except the original bit pattern).

Group the original bit patterns and all the first and second neighbor bit patterns into a three-tuple format.

Reorganize the three-tuples as pairs with the same original patterns and the same second neighbor bit patterns.

Next Page

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Original Three-Tuple Test Patterns

Reducing Mechanism

Reduced Three-Tuple Test Patterns

Inject the original bit patterns and the second neighbor bit patterns of the reduced three-tuple set into the test circuit.

END
Illustration of the Two-Input Change Test Patterns

**Two-Input Change:**

(a) 3-variable case:

For the first move, the starting cell has three neighbors. Then, at the second move, the second cell has two neighbors. So, the total number of patterns:

\[ 8 \times (1 \times 3 \times 2) = 48 \text{ patterns} \]

(b) 4-variable case:

For the first move, the starting cell has four neighbors. Then, at the second move, the second cell has three neighbors. So, the total number of patterns:

\[ 16 \times (1 \times 4 \times 3) = 192 \text{ patterns} \]

In general, the total number of the original three-tuple test patterns for \( N \) inputs:

\[ 2^N \times N \times (N - 1) \]

Illustration of the Reducing Mechanism

**STATE_VALUE_TABLE**

<table>
<thead>
<tr>
<th>Input Pattern</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
</tr>
<tr>
<td>001</td>
<td>1</td>
</tr>
<tr>
<td>010</td>
<td>1</td>
</tr>
<tr>
<td>011</td>
<td>0</td>
</tr>
<tr>
<td>100</td>
<td>1</td>
</tr>
<tr>
<td>101</td>
<td>1</td>
</tr>
<tr>
<td>110</td>
<td>0</td>
</tr>
<tr>
<td>111</td>
<td>1</td>
</tr>
</tbody>
</table>

**Original Three-Tuple Test Patterns**

- Table Look Up

**Reduced Three-Tuple Test Patterns**

- Table Look Up
Flow Chart of the Three-Tuple Test Pattern Reducing Mechanism

Start
Input Specification
Number of Inputs
Generate a range of naturals from: \{0, 1, 2, 3, ..., 2^n - 1 \}
Natural to BIT_VECTOR
Each input logic value is injected into the test circuit.
Each input logic value and its corresponding output logic value are memorized into a tabular form.
Original Three-Tuple Test Patterns
STATE_VALUE_TABLE
Reducing Mechanism
Reduced Three-Tuple Test Patterns

Flow Chart for the Hazard Detection Algorithm

Start
Static 0 ?
Yes -> Assertion Message
No
Static 1 ?
Yes -> Assertion Message
No
Dynamic 0 ?
Yes -> Assertion Message
No
Dynamic 1 ?
Yes -> Assertion Message
No
Function 0 ?
Yes -> Assertion Message
No
Function 1 ?
Yes -> Assertion Message
No
Next Input Pattern Pair
Methodology for Individual Hazard Detection

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>Output Event Counting from (first input pattern, second input pattern)</th>
<th>Output Condition Matching</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static 0 Hazard</td>
<td>Single-Input Change (1, 2)</td>
<td>&quot;0000&quot; when the present output is 'X'</td>
</tr>
<tr>
<td>Static 1 Hazard</td>
<td>Single-Input Change (1, 2)</td>
<td>&quot;0100&quot; when the present output is 'X'</td>
</tr>
<tr>
<td>Dynamic 0 Hazard</td>
<td>Single-Input Change (1, 3)</td>
<td>&quot;1000&quot; when the present output is 'Y'</td>
</tr>
<tr>
<td>Dynamic 1 Hazard</td>
<td>Single-Input Change (1, 3)</td>
<td>&quot;0010&quot; when the present output is 'Y'</td>
</tr>
<tr>
<td>Function 0 Hazard</td>
<td>Two-Input Change (1, 2)</td>
<td>&quot;0101&quot; when the present output is 'X' and the hazard information does not match with the static hazard information</td>
</tr>
<tr>
<td>Function 1 Hazard</td>
<td>Two-Input Change (1, 2)</td>
<td>&quot;1011&quot; when the present output is 'X' and the hazard information does not match with the static hazard information</td>
</tr>
</tbody>
</table>

1 The static hazard information includes:
   a. The first input combination that causes the static hazard
   b. The second input combination that causes the static hazard
   c. The amount of time between the second input combination and the first output event that is caused by that input combination
   d. The pulse width of the static hazard glitch
--- VHDS Report Summary for the Single-Input Change Hazard Analysis

Test Circuit Statistics:
Number of Primary Inputs: 3
Minimum Propagation Delay of the test circuit with respect to F: 4 NS
Maximum Propagation Delay of the test circuit with respect to F: 6 NS

----------------------------- VHDS Report Summary -----------------------------

Static 1 hazard is detected at 
559 NS 111
565 NS 110
563 NS 1 F
569 NS 0 F
571 NS 1 F

--- VHDS Report Summary for the Two-Input Change Hazard Analysis

Test Circuit Statistics:
Number of Primary Inputs: 3
Minimum Propagation Delay of the test circuit with respect to F: 4 NS
Maximum Propagation Delay of the test circuit with respect to F: 6 NS

----------------------------- VHDS Report Summary -----------------------------

Function 0 hazard is detected at 
62 NS 000
68 NS 101
66 NS 0 F
72 NS 1 F
74 NS 0 F

--- VHDS Report Summary for the Two-Input Change Hazard Analysis

Test Circuit Statistics:
Number of Primary Inputs: 3
Minimum Propagation Delay of the test circuit with respect to F: 4 NS
Maximum Propagation Delay of the test circuit with respect to F: 6 NS

----------------------------- VHDS Report Summary -----------------------------

Function 0 hazard is detected at 
62 NS 000
68 NS 101
66 NS 0 F
72 NS 1 F
74 NS 0 F

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Function 0 hazard is detected at 
62 NS 000
68 NS 101
66 NS 0 F
72 NS 1 F
74 NS 0 F

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Maximum Propagation Delay of the test circuit with respect to F: 6 NS

----------------------------- VHDS Report Summary -----------------------------

Function 0 hazard is detected at 
62 NS 000
68 NS 101
66 NS 0 F
72 NS 1 F
74 NS 0 F
Logic Realization of the Sample Test Circuits

Summary of the Real Time Required for the Sample Test Circuits

Real Time Required (in Seconds)

<table>
<thead>
<tr>
<th>Number of Inputs</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>STATIC</td>
<td>71.3</td>
<td>131.6</td>
<td>198.4</td>
<td>504.3</td>
</tr>
<tr>
<td>FUNCT</td>
<td>68.2</td>
<td>157.8</td>
<td>227.5</td>
<td>548.7</td>
</tr>
<tr>
<td>STATIC + FUNCT</td>
<td>139.5</td>
<td>289.4</td>
<td>425.9</td>
<td>1,053.0</td>
</tr>
</tbody>
</table>
Table 1. Summary of the Hazards Found in the Test Circuits

<table>
<thead>
<tr>
<th>Circuit Model</th>
<th>Static 0 Hazard</th>
<th>Static 1 Hazard</th>
<th>Dynamic 0 Hazard</th>
<th>Dynamic 1 Hazard</th>
<th>Function 0 Hazard</th>
<th>Function 1 Hazard</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-INPUT CIRCUIT</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4-INPUT CIRCUIT</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>7</td>
<td>14</td>
</tr>
<tr>
<td>5-INPUT CIRCUIT</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>6-INPUT CIRCUIT</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
<td>13</td>
<td>2</td>
</tr>
<tr>
<td>4-INPUT CIRCUIT</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 2. Summary of the Real Time (Minutes) and Test Patterns Required for the Test Circuits

<table>
<thead>
<tr>
<th>Circuit Model</th>
<th>STATIC</th>
<th>FUNCT</th>
<th># of Single-Input Change Test Patterns</th>
<th># of Reduced Test Patterns for Two-Input Change Hazard Analysis</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-INPUT CIRCUIT</td>
<td>1.19</td>
<td>1.14</td>
<td>24</td>
<td>8 (24)</td>
</tr>
<tr>
<td>4-INPUT CIRCUIT</td>
<td>2.19</td>
<td>2.63</td>
<td>64</td>
<td>48 (96)</td>
</tr>
<tr>
<td>5-INPUT CIRCUIT</td>
<td>3.21</td>
<td>3.79</td>
<td>160</td>
<td>76 (320)</td>
</tr>
<tr>
<td>6-INPUT CIRCUIT</td>
<td>8.41</td>
<td>9.15</td>
<td>384</td>
<td>146 (900)</td>
</tr>
<tr>
<td>4-INPUT CIRCUIT</td>
<td>1.05</td>
<td>1.21</td>
<td>64</td>
<td>30 (96)</td>
</tr>
</tbody>
</table>

where STATIC is the real time (in Minutes) required for the Single-Input Change Hazard Analysis.

FUNCT is the real time (in Minutes) required for the Two-Input Change Hazard Analysis.

1 This 3 input circuit was发生变化 for dynamic hazard.

Conclusion

- Report common types of hazards.
- Predict all input combinations that cause the hazards.
- The VHDS works with any combinational circuit of any size.
- The VHDS is able to compute the minimum and maximum propagation delays of any logic circuit that is described structurally in VHDL.